A NEW DIFFERENTIAL DIFFERENCE CURRENT CONVEYOR BASED VARIABLE FREQUENCY OSCILLATOR ADJUSTABLE WITH A GROUNDED RESISTOR

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ABSTRACT

A current mode variable frequency sinusoidal oscillator employing single differential difference current conveyor is proposed. The circuit uses two capacitors and three resistors which are minimum in number. The frequency of oscillation can be adjusted by a grounded resistor without disturbing the oscillation condition. The presented topology was synthesized using an innovative genetic algorithm. PSPICE simulation results which confirm the theoretical analysis are included.

I. INTRODUCTION

Sinusoidal oscillators have a wide range of application in telecommunications, signal processing circuits, control and measurement systems. In the literature, several current mode active-RC oscillator circuits have been proposed which use single active element such as operational transconductance amplifier, current conveyor, current feedback amplifier and four terminal floating nullor [1-4]. Recently, a new building block called differential difference current conveyor (DDCC) was introduced [5], which gives further possibilities to the designers in analogue circuits. In this paper, a new single DDCC based current mode variable frequency sinusoidal oscillator is proposed. The realization is canonic as the oscillator uses two capacitors and minimal as it employs three resistors one of which is for achieving the variable frequency property. It also utilizes single active element that provides low power consumption. The oscillation frequency is controlled by a grounded resistor. The presented topology indicates that DDCC is a versatile building block to implement canonic current mode oscillators and does not need any additional output current terminal as opposed to some of the circuits in the literature [6, 7]. One such oscillator topology has been proposed earlier using DDCC [8], but it does not provide grounded resistor frequency control. Grounded resistor control leads to easier realization of grounded voltage-controlled resistance and integration. This makes realization of voltage-controlled oscillator easy [9].

The presented oscillator was synthesized using an innovative genetic algorithm discussed in detail in [10]. The employed genetic algorithm searches for topologies of a sinusoidal oscillator using a given active element, a DDCC in the present case, and finally gives the topology and characteristic equation of the oscillator in terms of resistor and capacitor values. However, the algorithm is incapable of ascertaining whether the complete set of topologies has been found. The final aim of the algorithm is to fully automate the synthesis and study of sinusoidal oscillators.

II. PROPOSED CURRENT MODE OSCILLATOR CIRCUIT

DDCC has the following characterizing equations:

$$I_{y1} = I_{y2} = I_{y3} = 0 \tag{1a}$$

$$V_x = V_{y1} - V_{y2} + V_{y3} \tag{1b}$$

$$I_z = I_x \tag{1c}$$

The proposed current mode variable frequency sinusoidal oscillator is shown in Figure 1. There is no need to use equation (1c) in the analysis of this circuit. The z-terminal of the DDCC is just used to take the output current.

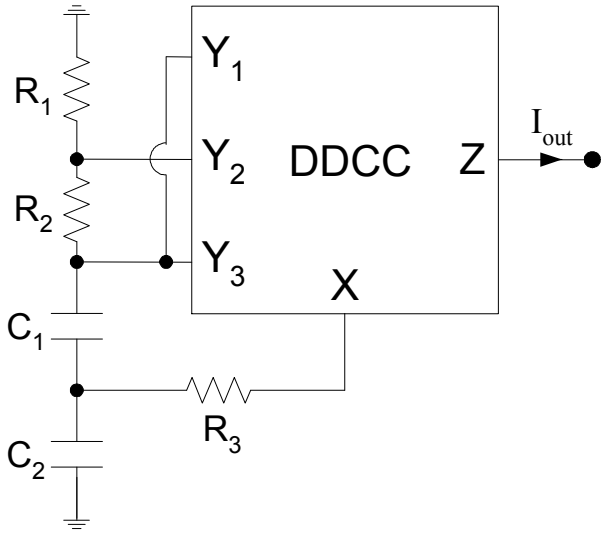

Figure 1. Proposed current mode variable frequency oscillator circuit

Routine analysis yields the oscillation condition and frequency as follows, respectively.

$$R_2 C_1 = R_3 (C_1 + C_2) \tag{2}$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{R_3 (R_1 + R_2) C_1 C_2}} \tag{3}$$

As it is seen in equations (2) and (3) the frequency of oscillation can be adjusted by the grounded resistor R_1 without disturbing the oscillation condition.

The sensitivity of the oscillation frequency to the passive element values can be found as follows.

$$S_{R_1}^{\omega_0} = -\frac{1}{2}\frac{R_1}{R_1 + R_2} \tag{4a}$$

$$S_{R_2}^{\omega_0} = -\frac{1}{2}\frac{R_2}{R_1 + R_2} \tag{4b}$$

$$S_{R_3}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2} \tag{4c}$$

As it is seen all passive element sensitivities are no more than one half in magnitude.

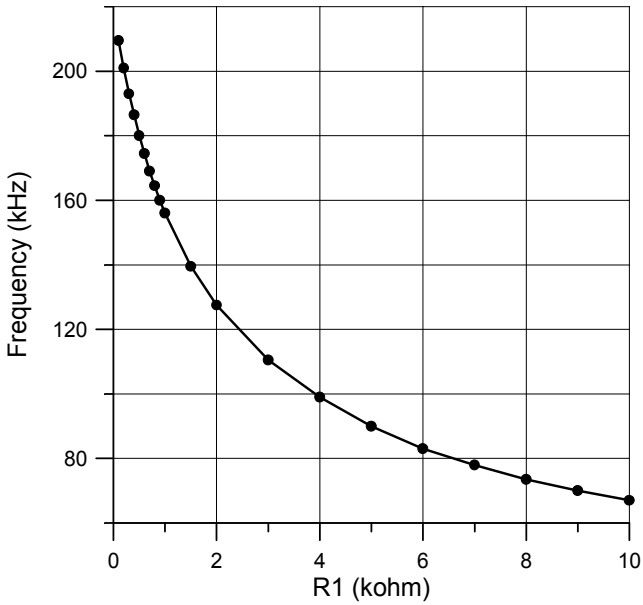

Figure 2. Simulated variation of oscillation frequency with the grounded resistor R_1

III. SIMULATION RESULTS

To verify the theoretical study, the oscillator circuit was simulated using PSPICE program on the basis of MIETEC 0.5um CMOS process parameters. In the simulation, passive components were chosen as R_1=0.1–10kΩ, R_2=1kΩ, R_3=0.5kΩ, C_1=C_2=1nF. The PSPICE simulations were performed using a CMOS realization of DDCC proposed in [11] with the same transistor aspect ratios and supply voltages (V_{DD}=2.5V and V_{SS}=-2.5V). The variation of oscillation frequency with the change in the value of R_1 is shown in Figure 2, which is in good agreement with the predicted theory.

IV. CONCLUSION

A single DDCC based current mode variable frequency sinusoidal oscillator employing minimum number of passive elements is presented. The oscillation frequency of the proposed circuit is adjustable by a grounded resistor without disturbing the condition of oscillation. All passive element sensitivities are no more than one half in magnitude. The oscillator circuit was synthesized using an innovative genetic algorithm. The presented topology indicates that DDCC is a versatile building block to implement canonic current mode oscillators and does not need any additional output current terminal. PSPICE simulation results are given to verify the theoretical analysis.

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