An Ultra Low-Voltage, Ultra Low-Power DTMOS-Based CCII Design for Speech Processing Filters

Atilla Uygur[1], Hakan Kuntman[2]

[1]Dept. of Electronics and Telecommunication Engineering, ITU Ayazaga Campus, 34469, Maslak-Istanbul, Turkey
uygura@itu.edu.tr
[2]Dept. of Electronics and Telecommunication Engineering, ITU Ayazaga Campus, 34469, Maslak-Istanbul, Turkey
kuntman@itu.edu.tr

Abstract

In this study, an ultra low-voltage, ultra low-power dynamic threshold voltage MOS transistor (DTMOS)-based CCII design has been presented. The proposed circuit operates under ±0.2 V symmetric power supply. Consisting of only eight transistors, it consumes only 214 nW power while all transistors are working in the subthreshold region. It has a 570 kHz 3 dB-bandwidth from X terminal to Y terminal for the voltage gain. TSMC 0.18 µm process technology is used in the design of CCII block which is then employed in a band-pass filter configuration. In order to further investigate its performance, real speech signals are fed to the filter and close agreement is found between theoretical study and simulated responses.

1. Introduction

In analog circuit design, current-mode circuits have the advantage of higher bandwidths than their voltage-mode counterparts due to current source driven low-impedance nodes that carry current signals. These low-impedance nodes lead to relatively high pole frequencies in comparison to voltage mode circuits [1]. Furthermore, since voltage signals are not mainly used in the signal processing, low-voltage circuits having higher bandwidths than voltage-mode alternatives can be realized more easily in the current-mode approach [2].

Parallel to the increase in portable electronic devices, power consumption has become an essential design specification and crucially important requirement for power-efficient circuits. First response to this requirement in digital designs is to reduce the supply voltage. This affects the overall circuits' dynamic power consumption which is proportional to square of supply voltage. However this approach has caused significant performance losses in analog circuits where the decrease in threshold voltages does not follow the same trend of power supply reduction due to the leakage problems [3-4]. Therefore, today's analog circuits, sharing same chip with their digital counterparts, suffer from the low-voltage levels of digital circuitry and relatively high threshold voltages which are not reduced below certain limits in standard CMOS process technology for keeping the leakage currents in acceptable ranges. This fact brings about the necessity of designing novel analog circuits that are suitable for low-voltage and low-power operation [5].

Current Conveyor is an important current-mode building block. Having three different generations, second generation current conveyor (CCII) is the mostly used one due to its versatile configurations. Although there are some CCII topologies for low-power and low-voltage operation [6], it is however difficult to find ultra low-power ultra low-voltage CCII designs having transistors operating in the subthreshold mode which is the optimum region for power saving when high frequency operation is not required.

In this study, a dynamic threshold voltage MOS transistor (DTMOS)-based CCII circuit is proposed. The transistors are all operating in the subthreshold region to maximize the power consumption efficiency. The proposed circuit is then employed as the active block in a band-pass filter configuration. The performance of this circuit is then shown in the processing of real human speech signals.

2. DTMOS Transistor

DTMOS transistor was first proposed by Assederaghi et al in their pioneering papers [7-8] for silicon on insulator (SOI) process technology. Although the idea goes back to earlier dates [9], these papers have best described the device and the underlying reasons of the operation.

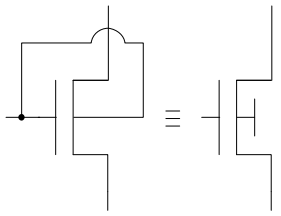

Fig. 1. DTMOS transistor and its commonly used circuit symbol

As shown in Fig. 1, the idea is to connect the gate and the body of a transistor to dynamically change its threshold voltage V_{TH} by utilizing the relation in (1) where ϕ_0 is the total surface band bending and γ is body effect factor. V_{SB} denotes the source to body voltage and V_{TO} is zero-V_{SB} bias threshold voltage. The equation is written for a long channel n-MOS transistor where drain-induced barrier lowering (DIBL) effect is neglected.

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right) \quad (1)$$

Zero-V_{SB} bias threshold voltage, V_{TO} is defined by

$$V_{TO} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0} \quad (2)$$

where V_{FB} is the flat band voltage and the body effect factor γ is given by

$$\gamma = \frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}} \tag{3}$$

where N_A is the substrate doping, ε_s represents dielectric permittivity of silicon and C_{ox} is the oxide capacitance for unit area. In (1), ϕ_0 is usually considered equal to two times Fermi potential $2\phi_F$ for simplicity. However, to obtain more accurate approximations, this should be calculated as in (4) where α is an experimental fitting parameter and ϕ_t is the thermal voltage [10-11].

$$\phi_0 = 2\phi_F + \alpha\phi_t \tag{4}$$

For conventional MOS operation, V_{SB} value is either zero or positive whereas in DTMOS operation this value might become negative, however, the equation in (1) is still applicable for not too large negative values provided that the junction currents are negligibly small [10-11].

One important problem of DTMOS configurations is the lateral bipolar transistor consisting of source body and drain body junctions which might latch up and cause very high body currents. This should be strictly kept under control for correct mechanism of the device. Thus, total supply voltage, chosen in this study, is low enough (0.4 V) to limit forward biased diode currents. It is practically shown in circuit realizations that forward biased diode currents do not effect much the operation of the transistor or the overall circuit if the supply voltages, in other words, forward body biases are close to 0.4 V~0.5 V [12-13]. The main reason is that the mobile carrier concentrations for supply voltages in 0.4 V~0.5 V range do not reach high levels in modern highly doped substrates leading to source body, drain body junctions with high turn-on voltages [10].

It is important to note that compact models such as EKV, BSIM are still valid for less than 0.4 V~0.5 V forward biased source body, drain body junctions even those models assume the total depletion approximation. Under these voltage levels, free carriers in the channel are so small in numbers that their effects can be safely neglected in the operation of long channel DTMOS devices [11, 14]. Therefore, we have used BSIM3v3.2 model for the transistors in the circuit and minimum channel lengths for DTMOS transistors are chosen as 2 µm to prevent short channel effects and for better modeling the device.

Subthreshold mode of operation of CMOS circuit is usually the preferred method for power-saving circuits if the high frequency operation is not needed. This is the chosen mode of operation in this study where ultra low-voltage, ultra low-power designs are focused on DTMOS transistors having inherent, close to ideal subthreshold swings. Moreover, DTMOS transistors with high on-off ratio have better drivability than a regular MOS transistor under ultra low-voltage operation which makes them suitable devices for ultra low-power, ultra low-voltage operations where transistors usually are operating in weak inversion region.

3. DTMOS-based CCII Circuit

DTMOS-based an ultra low-voltage, ultra low-power, subthreshold CCII circuit in Fig. 2, has been proposed in this study. Since ±0.2 V supply voltages are used, total bias voltage over the source body and drain body junctions of DTMOS transistors limits the excess diode currents, prevents latch-up and do not disturb normal transistor operation.

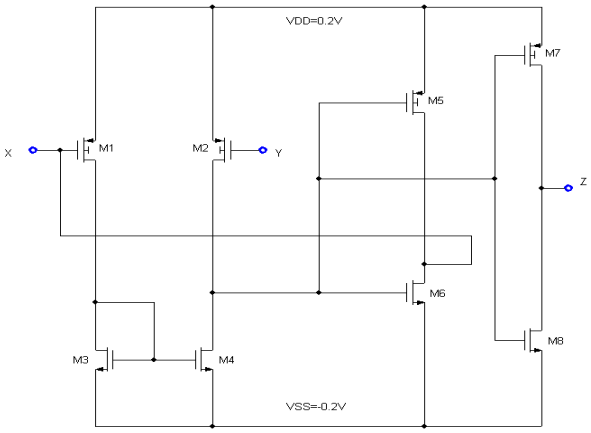

Fig. 2. DTMOS-based ultra low-voltage, ultra low-power subthreshold CCII circuit

In the proposed CCII circuit, TSMC 0.18 µm process parameters are used. All transistors are operating in the subthreshold region which is the best region for power saving applications. Additionally, the circuit consists of only eight transistors which increase the power consumption efficiency of the design and minimize the parasitics as well. The input stage is formed by a pseudo-differential low-voltage amplifier consisting of M1-M4. The output stage is the class AB stage from [6] with the modification of DTMOS transistor usage for ultra low-voltage operation. M1-M2 and M5, M7 are the p-MOS DTMOS transistors. There is feedback in the topology including M6 transistor which helps to decrease the resistance at the X input terminal which should be zero ideally. However, this is very difficult to achieve under subthreshold mode of operation where transistor transconductances are significantly low which severely affects the resistance seen at the X terminal.

From Table 1, it can be concluded that relatively large transistors are used in the design. They are chosen for correct operation of the circuit under ultra low supply voltage. This is generally the expected case for any MOS circuits operating in the subthreshold region where transistor dimensions have been chosen large to enable the flow of targeted current under low-voltage operation.

Table 1. Transistor dimensions of the proposed CCII

Transistor	Width	Length
M1, M2, M5,M7	300 µm	2 µm
M3, M4	50 µm	2 µm
M6, M8	320 µm	0.4 µm

The circuit is simulated by the program SPICE. Fig. 3 shows the input range where the V_X voltage follows V_Y voltage. From the figure, it can be said that the input voltage range is ±60 mV with small following error. Defining a relative error term as

$$\varepsilon = \frac{|v_x - v_y|}{v_x} \tag{5}$$

The percentage of this error is found as less as 0.2% between ±60 mV input range as shown in Fig. 4.

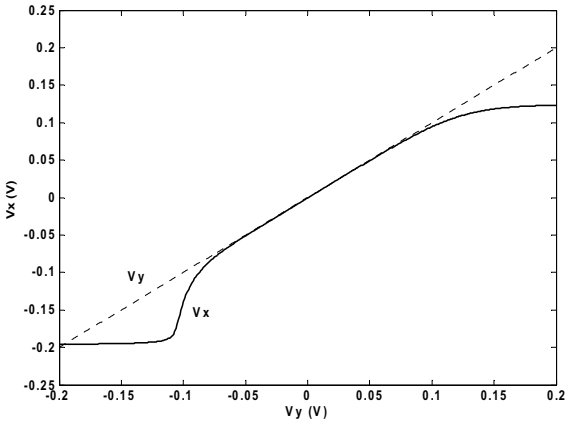

Fig. 3. The change of V_X voltage versus V_Y voltage

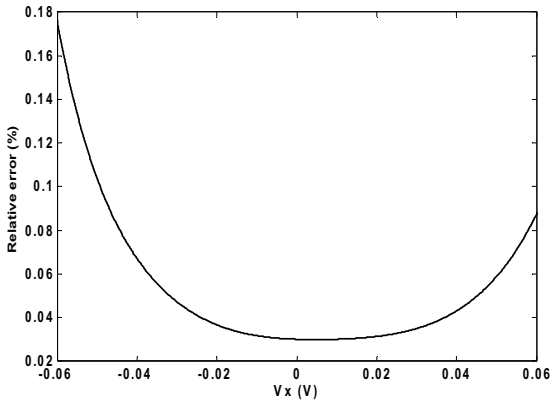

Fig. 4. The relative error percentage of V_X voltage while following V_Y input voltage

Neglecting the output resistances of transistors, the error term can approximately be calculated from the circuit as in (6). Thus matching the transconductances of M1 and M2; M3 and M4 minimizes this error term.

$$\varepsilon = \frac{\left| g_{m2}g_{m3} - g_{m1}g_{m4} \right|}{g_{m2}g_{m3}} \tag{6}$$

Fig. 5 depicts the sinusoidal response obtained by applying 80 mV peak to peak V_Y input voltage.. Frequency response of V_X and V_Z is illustrated in Fig. 6 when an input AC signal is applied to the Y terminal. It is found that the 3 dB-bandwidth of V_X and V_Z voltages is close to 600 kHz which is quite sufficient for sound frequency applications. From Fig. 6, 3 dB-frequency of V_X/V_Y gain is found as 570 kHz.

The performance summary of the proposed CCII circuit has been tabulated in Table 2. In the table, another low-voltage low-power, bulk-driven current conveyor circuit from the study in [15] is compared with this work. A Figure of Merit (FOM) is developed as a metric to evaluate overall performances more easily. In (7), V_{swing_ratio} is the ratio of total input voltage swing to whole supply voltage. $f_{3\,dB}$ is the 3 dB-frequency of V_X/V_Y voltage gain. *VDD* is the supply voltage and *Power* is the total quiescent power consumption of the circuit.

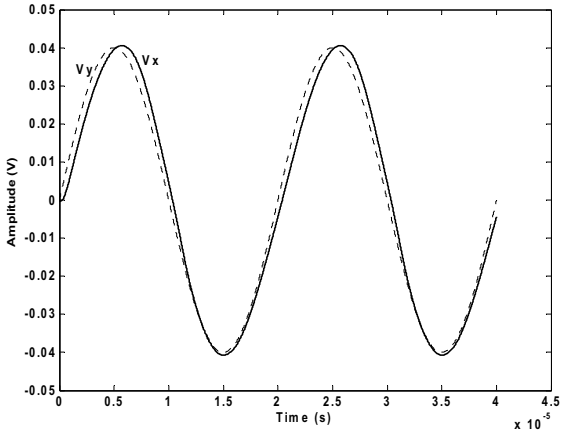

Fig. 5. The sinusoidal response of V_X and V_Y voltages

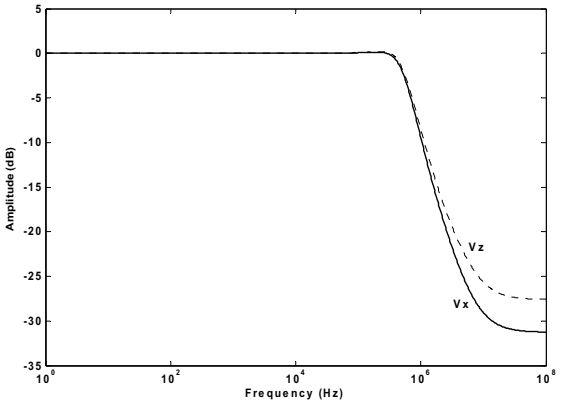

Fig. 6. Frequency response of V_X and V_Z voltages

$$FOM = \frac{V_{swing\_ratio} \times f_{3\,dB}}{VDD \times Power} \tag{7}$$

It can be figured out that for better performance, higher FOM value is desired. In Table 2, the proposed CCII achieves almost eight times higher FOM value than [15] which is a significant improvement.

Table 2. Performance summary of the proposed CCII

Current Conveyor	[15]	This Work
Technology	TSMC 0.18 µm	TSMC 0.18 µm
Supply Voltage	±0.4 V	±0.2 V
Input Voltage Range	-380 mV - +380 mV	-60 mV - +60 mV
3 dB-Bandwidth (V_X/V_Y)	14 MHz	570 kHz
Power Consumption	64 µW	0.21 µW
V_Y resistance@1 kHz	272 GΩ*	11.8 MΩ
V_X resistance@1 kHz	27Ω*	964 Ω
V_Z resistance@1 kHz	0.89 MΩ*	2 MΩ
FOM (10^{12})	0.259	2.035

*Resistances in [15] were measured for frequency in kHz range not specifically at 1 kHz.

4. CCII-based Band-pass Filter for Speech Processing

The proposed DTMOS-based subthreshold current conveyor is used in a band-pass filter configuration which is given in the reference [16]. This filter configuration is shown in Fig. 7. The reason for choosing a band-pass filter type is that in analog hearing aid systems, there are analog filter banks that consist of band-pass filters [17]. These filters should be capable of operating at sound frequencies with very little power consumption to save the life of the battery used in the hearing aid system.

The filter circuit employing the proposed CCII was simulated by program SPICE and the frequency response in Fig. 8 is obtained when the passive element values of C_1=628 pF, C_2=628 pF, R_1=100 kΩ and R_2=100 kΩ are used.

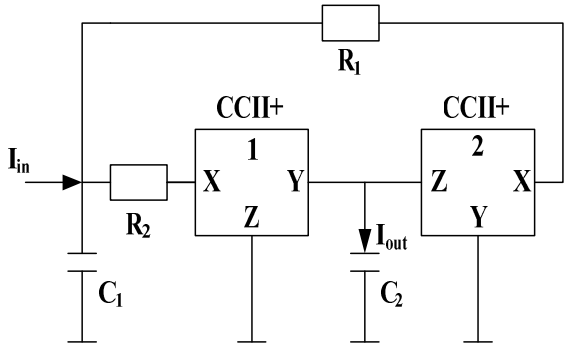

Fig. 7. CCII based band-pass filter [16]

The pole frequency and quality factor of the filter is given in (8). They are adjusted to example values of close to 2.5 kHz pole frequency and Q value of 1/2 which shows that the circuit behaves close to the ideal one throughout the sound frequency range and it might be employed in low-power and low-voltage analog hearing aid filter banks.

$$\omega = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \quad Q = \frac{\sqrt{R_1 R_2}}{R_1 + R_2}\sqrt{\frac{C_1}{C_2}} \tag{8}$$

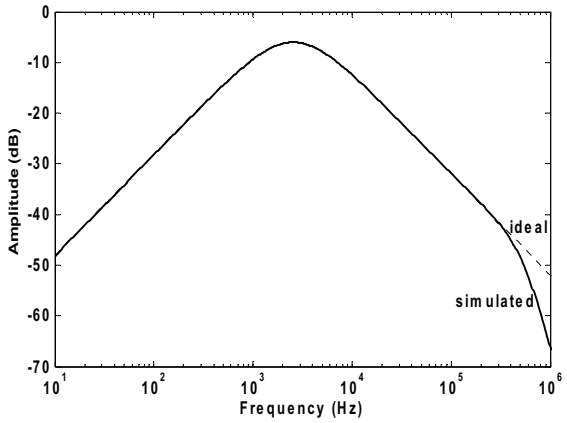

Fig. 8. Ideal and simulated filter amplitude response with respect to frequency

Fig. 9 is obtained for a peak to peak 80nA input sinus current signal for the filter circuit where the amplitude of the output is the half of that of output. This is caused by the half gain characteristic of the band-pass filter in Fig. 7 which can be also seen from Fig. 8.

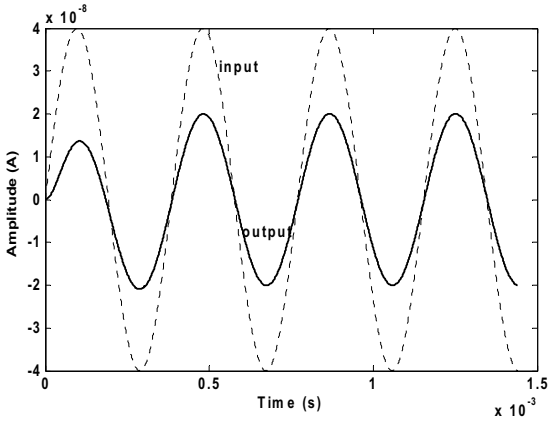

Fig. 9. Sinusoidal characteristics of input and output of the filter

Total harmonic distortion of the filter with respect to peak to peak input current signal is depicted in Fig. 10. From the figure, it is seen that for input current signals not exceeding peak to peak 4 μA, THD is less than 2.5 %. To note that, this value has been achieved using only ±0.2 V supply voltage while consuming only 428 nW total power for overall filter circuit.

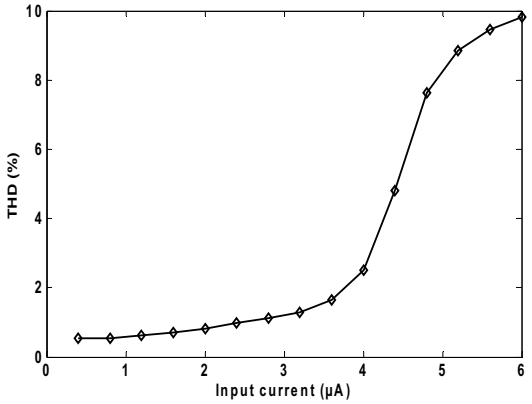

Fig. 10. Total harmonic distortion of the filter Transient response of input and output of the filter

To further investigate the characteristics of the CCII-based filter and its suitability for hearing aid applications, real human speech signal is applied to the filter in SPICE as input, then ideal and simulated filter responses are compared. Fig. 11 shows author's speech signal while saying the word "DTMOS".

Fig. 12 is the ideal and simulated filter responses for input speech signal while saying the word "DTMOS". For clarity, only the response of the interval between 3 ms and 5 ms is shown in the figure. As it is illustrated in the figure, resulting ideal and simulated responses are close to each other which show the suitability of the proposed CCII circuit for speech processing filters.

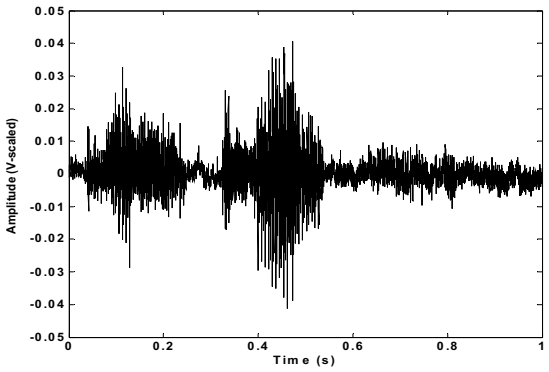

Fig. 11. Input speech signal while saying the word "DTMOS"

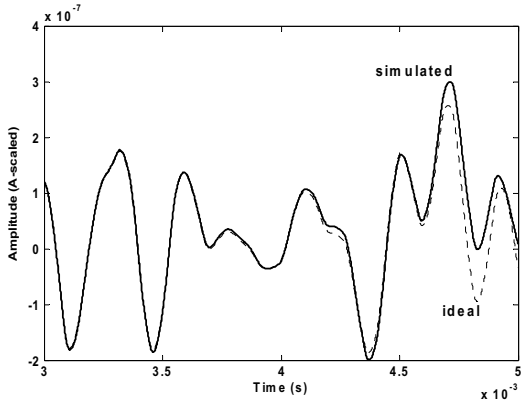

Fig. 12. Ideal and simulated filter response to input speech signal

5. Conclusions

In this paper, using DTMOS transistors, having close to ideal subthreshold swings, an ultra low-voltage and ultra low-power subthreshold CCII is proposed. Its performance is investigated with SPICE simulations. The proposed current conveyor is then employed in a band-pass filter topology to show its suitability for sound frequency range of operation and speech processing applications. Theoretical and simulated results are found in close agreement. The importance of the design is that, under only ±0.2 V supply voltage and consuming very low power, half of MHz range operation has become possible with using only eight transistors thanks to the usage of DTMOS transistors and current-mode approach. The circuit is compared with available literature and the proposed circuit is found performing significantly better than its bulk-driven alternative. To the best knowledge of authors, the proposed circuit in this study consists of least number of transistors in a DTMOS-based CCII circuit in the literature that is able to operate under ±0.2 V supply voltages using standard CMOS process technology.

6. References

[1] C. Tomazou, F. J. Lidgey, D. G. Haigh, "Analogue IC design: the current-mode approach" Peter Peregrinus, London, England, 1990.

[2] A. Uygur, H. Kuntman, "Seventh order elliptic video filter with 0.1dB pass band ripple employing CMOS CDTAs" *AEÜ International Journal of Electronics and Communications*, vol. 61, pp. 320-328, 2007.

[3] Y. Berg, "Ultra low-voltage CMOS transconductance amplifiers", *Analog Integrated Circuits and Signal Processing*, vol. 73, no. 3, pp. 683-692, 2012.

[4] Y. Berg, O. Mirmortahari, "Ultra low-voltage CMOS current mirrors" *Analog Integrated Circuits and Signal Processing,* vol. 68, no. 2, pp. 219-232, 2011.

[5] A. Uygur, H. Kuntman, "DTMOS-based 0.4V ultra low-voltage, low-power VDTA design and its application to EEG data processing", *Radioengineering*, vol. 22, no.2, pp. 458-466, 2013.

[6] Ferri G., Guerrini, N.C, "Low-voltage low-power CMOS current conveyors", Kluwer Academic Publishers, Netherland, 2003.

[7] F. Assaderaghi, S.A Parke, D. Sinitsky, J. Bokor, P.K. Ko, C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for very low-voltage operation" *IEEE Electronic Device Letters*, vol. 15, no.12, pp.510-512, 1994.

[8] F. Assaderaghi, D. Sinitsky, S.A. Parke, J. Bokor, P.K. Ko, C. Hu, "Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low-voltage VLSI" *IEEE Transactions on Electron Devices*, vol. 44, no. 3, pp. 414-422, 1997.

[9] J.P. Colinge, "An SOI voltage-controlled bipolar-MOS device" *IEEE Transactions on Electronic Devices* vol. ed-34, pp. 845-849, 1987.

[10] Y. Tsividis, C. McAndrew, "Operation and modelling of MOS transistor", Oxford University Press, New York, USA. 2011.

[11] F.J De La Hidalga-W, M.J. Deen, E.A. Gutierrez-D, F. Balestra, "Effect of the forward biasing the source-substrate junction in n-metal–oxide–semiconductor transistors for possible low power complementary metal–oxide–semiconductor integrated circuits' applications" *Journal of Vacuum Science Technology B*, vol. 16, no. 4, pp. 1812-1817, 1998.

[12] S. Mohammadi, C.R Seivakumar, "Calculation of depletion layer thickness by including the mobile carriers" *IEEE Transactions on Electronic Devices,* vol. 43, no.1, pp.185-188, 1996.

[13] A. Srivastava, "Back gate bias method of threshold voltage control for the design of low-voltage CMOS ternary logic circuits" *Microelectronics Reliability,*vol. 40, p.2107-2110, 2000.

[14] J.P. Colinge, J.T. Park, "Application of the EKV model to the DTMOS SOI transistor" *Journal of Semiconductor Technology and Science*, vol. 3, no. 4, pp. 223-226, 2003.

[15] F. Khateb, N. Khatib, D. Kubanek, "Novel low-voltage low-power high-precision CCII± based on bulk-driven folded cascode OTA" *Microelectronics Journal,* vol. 42, no. 6, pp. 622-631, 2011.

[16] A. Fabre, H. Amrani, O. Saaid, "Current-mode band-pass filters with Q-magnification" *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 43, no. 12, pp. 839-842, 1996.

[17] D.C. Salthouse, R. Sarpeshkar, "A practical micropower programmable band-pass filter for use in bionic ears" *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1. pp. 63-70, 2003.