A Novel rectifier/inverter with adjustable power factor

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Abstract - An adjustable power-factor operation of a boost-based bidirectional ac/dc converter is described. It possesses a bi-directional power flow capability. The converter has a bias capacitor connected in series with the ac source which provides a dc voltage boost at the input. By appropriate control of the bias capacitor dc voltage, an always positive voltage is applied to the input of a boost power-factor corrector. This enables removal of a diode bridge rectifier that is commonly employed in switch-mode rectifiers. A bi-directional dc/dc boost converter allows for power factor adjustment in the full range of 0°–360°. Hence, the circuit can be used to compensate reactive power of other loads while either consuming active power (as in a battery charger) or providing active power (as in photovoltaic systems). The total harmonic distortion of the converter input current is less than 1.2% for any mode of operation. The operational principle of the proposed circuit was verified by Saber simulations.

I. INTRODUCTION

Since most of industrial and many residential loads are of inductive type (e.g., induction motors), the problem of compensating reactive power flow has been researched for several decades. Traditionally, reactive power compensation is addressed in terms of power factor improvement capacitors. Later on, static VAR control was introduced and its superiority was proven in terms of price, bulkiness, and the flexibility to adjust and precisely compensate for a variable power factor of the load. [1], [2]. A search for better power factor correction (PFC) circuits became a challenge for many researchers and engineers for the past two decades. Indeed, various topologies were found suitable for PFC circuits [3], [4]. All switch-mode PFC circuits share a common operation principle: by means of a feedback control loop, the converter input average current is forced to follow the input voltage, emulating a resistive input characteristic R_e [5]. Usually, the switching dc/dc converter is capable of handling only positive input current and requires a positive input voltage. Therefore, a diode bridge rectifier interfaces the switching converter with the ac supply [6]. Evidently, this arrangement allows for a unidirectional power flow, i.e., the converter always consumes power at its input. In this paper, it is proposed to employ
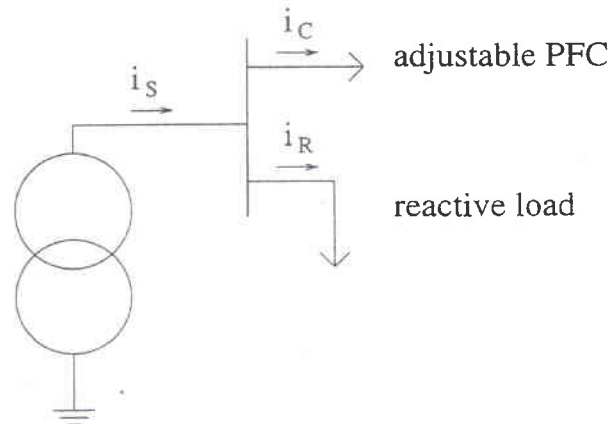

Fig. 1. Reactive power compensation with an active PFC.

a high power factor rectifier [7], not only for rectification that does not produce harmonics but also to compensate for non-unity power factor of other loads. For this to be possible, a switch-mode rectifier capable of bidirectional power transfer must be used. Although other bidirectional switch-mode rectifiers exist (such as the half bridge boost rectifier), a new type of a rectifier is suggested herein. It was found that the proposed topology can operate with any phase shift. By continuous control of the phase, optimal VAR compensation is possible, i.e., the converter will present a reactive characteristic which precisely cancels with that of other loads. The voltage source will supply only active current. Improved efficiency and power factor are also expected as a result of omission of the diode rectification bridge. The theoretical derivation are validated with Saber simulator.

The schematic idea of the reactive power compensation with an active PFC is shown in Fig. 1. Sinusoidal currents i_R and i_C are shifted with respect to the mains voltage by angles θ and ϕ, respectively.

$$i_R(t) = I_r sin(\omega t + \theta) \qquad (1)$$

$$i_C(t) = I_c sin(\omega t + \phi). \qquad (2)$$

To achieve phase compensation the following relationships must be fulfilled
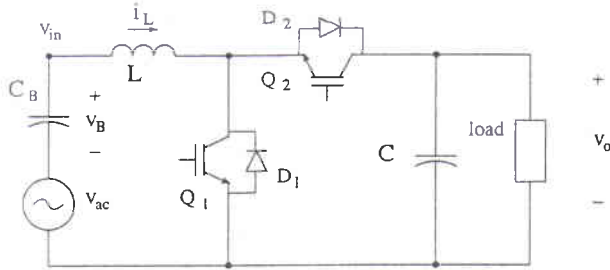
$$Q_c = -Q_r \qquad (3)$$

Fig. 2. Topology of the converter power stage.

$$\phi = -sin^{-1}(\frac{I_r}{I_c}sin\theta) \tag{4}$$

$$I_c = \frac{P_c}{V cos\phi} \approx \frac{P_{out}}{\eta V cos\phi} \tag{5}$$

where Q denotes reactive power, P_c and P_{out} are the input and output active powers of the PFC, and η is the converter efficiency.

II. Converter Operation

The power stage of the proposed converter is depicted in Fig. 2. The ac power source is coupled to a switch via an inductor and a capacitor. The load can be either passive or active (e.g., a switching post-regulator). As it can be seen, the four-diode bridge rectifier that commonly couples the ac source and the switching converter does not exist in this topology. This results in a possibility to reverse the direction of the inductor current. The output voltage v_o is positive. Therefore, the input voltage v_i must be positive as well. A second reason requiring an always positive input voltage is the use of switches with unidirectional voltage blocking capability. It is the role of the bias capacitor C_B to levitate v_i to an always positive value.

Thus, the boost part of the converter (consisting of the inductor, the single pole double through (SPDT) and the dc link capacitor C) practically couples two positive voltages and may, therefore, be implemented by semiconductor switches. Since the circuit is to shape the input current to be closely sinusoidal, these switches must be able to conduct in both directions. Before the IGBTs in Fig. 2 can be controlled in the appropriate manner to produce the desired input current, both capacitors C_B and C must be charged up to steady state values $v_{C_B}(0)$ and V_o ($v_{C_B}(0)$ designates the initial voltage of the bias capacitor when steady state operation begins). Once the capacitors are charged to the steady state values of voltage, the following switching sequence is applied: the IGBTs Q_1 and Q_2 may be driven by complimentary signals, however, only one IGBT will conduct during each line cycle, while the inductor current is alternately diverted from one IGBT to the antiparallel diode of the second IGBT and vice versa. This is best seen in Fig. 3 where the conduction modes are presented.

Since the inductor current, that is the input current, must follow the line voltage shape, the current is positive during the positive half-cycle of the line and negative during the negative half-cycle. During the positive half period of the line voltage the converter operates in mode 1, alternately switching between states 1-a and 1-b (Fig. 3). In this mode, power is transferred from the line voltage source and from the bias capacitor C_B to the dc output while the average input current $< i_L >$ follows v_{ac}. During the negative half-cycle the converter operates in mode 2 alternately switching between states 2-a and 2-b (Fig. 3) and drawing power from the output capacitor C. The average input current $< i_L >$ again follows v_{ac}. Thus, the power drawn from the line and v_o charges the bias capacitor. In states 1-a and 2-a the inductor voltage is positive, resulting in an increasing current for any v_{ac}, while in states 2-a and 2-b this voltage is negative, resulting in a current that decreases for any v_{ac}. This indicates that the input current can be controlled by alternately switching between states a and b to produce the desired current shape. Specific conditions that guarantee controllability of the input current and the resulting constrains implied on the power stage are derived in the next section.

III. Power Stage Design

The major objective of the converter is to supply a sinusoidal current with phase and amplitude given by (4) and (5). A suitable reference current signal i_{ref} must be generated by a controller

$$i_{ref} = I_{ref}sin(\omega t + \theta). \tag{6}$$

The converter is controlled in such a manner that the inductor average current $< i_L >$ follows the reference current.

$$< i_L(t) >= \frac{1}{T_s} \int_t^{t+T_s} i_L(\tau)d\tau, \tag{7}$$

$$< i_L(t) >\approx i_{ref} \tag{8}$$

Let us calculate the resulting input voltage v_i by applying KVL at the input loop of the converter of Fig. 2.

$$v_i(t) = v_{ac}(t) + v_{C_B}(t)$$

$$= v_{ac}(t) - \frac{1}{C_B} \int_0^t i_C(\tau)d\tau + v_{C_B}(0) \tag{9}$$

As the switching frequency is much higher than the ac line frequency, $< i_L >$ may be replaced with i_L. Assuming that the control operates as it is intended to, $< i_L >$ closely approximates i_{ref}. Thus, substitution of i_{ref} from (6) into (9) yields v_i:

$$v_i(t) = V sin(\omega t) + v_{C_B}(0) + \frac{I_c}{\omega C_B}[cos(\omega t + \phi) - cos\phi] \tag{10}$$

The converter should be designed in such a way that $v_i(t)$ is always positive.

Like in all boost converters, the value of the inductor L is derived primarily from the allowable ripple of the input current and that of the dc link capacitor mainly by the

mode 1 (positive half-cycle)
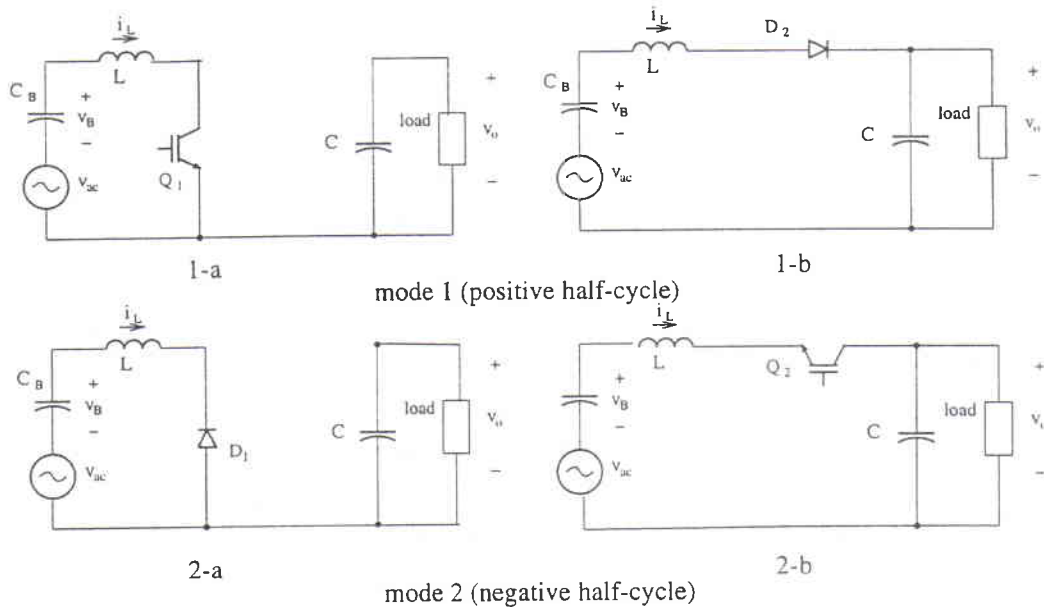
mode 2 (negative half-cycle)

Fig. 3. Two modes of operation during rectification.

allowable output voltage fluctuation. In PFC circuits, however, it is required to evaluate this components against the dynamics of the converter to ensure its ability to obey the control command and carry out the desired current tracking. It can be seen in Fig. 2 that the controllability of the input current is not guaranteed for arbitrary circuit parameters. For instance, if $v_o < v_1$, a decreasing input current cannot be produced. Likewise, if the inductor L is to large, the slope of i_L during the on state might not be sufficient in order for the current i_L to track the reference i_{ref}. Thus, the power stage might put limits on the current tracking, regardless of the control method. In addition, the value of the bias capacitor C_B needs to be determined. The input current can be controlled to follow the reference current if two conditions are met: (a) the inductor current slope in state a (Fig. 3) is greater than the reference current slope, and (b) the inductor current slope in state b (Fig. 3) is smaller than the reference current slope.

$$\left.\begin{array}{ll} \text{(a)} & \frac{di_L(t)}{dt}\Big|_{(s=1)} > \frac{di_{ref}}{dt} \\ \text{(b)} & \frac{di_L(t)}{dt}\Big|_{(s=2)} < \frac{di_{ref}}{dt} \end{array}\right\} \quad \text{for every } t. \qquad (11)$$

If this condition is met, distortions associated with the ac voltage zero crossing can be eliminated. These distortions are inevitable in a conventional APFC with a diode rectifier at the front end. The simulation schematic of the compensation system with control scheme is shown in Fig. 4. In order to save simulation time, the reactive load is modeled as a current source with a predetermined power factor. The PFC input current is shaped with a hysteretic controller.

IV. SIMULATION RESULTS

The simulations were performed for both active and passive loads to the PFC (Fig. 4 shows the passive load case).
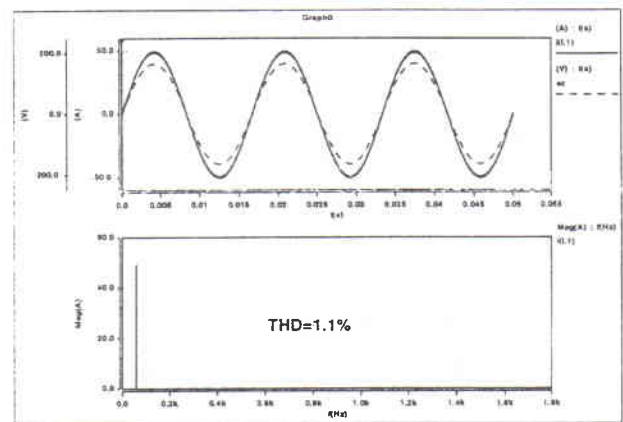

Fig. 5. Operation of the PFC at $\phi = 0°$. Top graph: current i_C (solid line) and mains voltage (dashed line). Bottom graph: THD of current i_C.

To demonstrate the operation of the circuit for the whole range of power factors, four critical values of the phase shift ϕ are shown. The converter operates at about 4 kVA input power. Fig. 5 presents operation of the converter with a unity power factor. Fig. 6 shows purely inductive operation. The inversion mode (which requires a source at the converter output) is presented in Fig. 7. The converter as a purely capacitive load is shown in Fig. 8. In all the case, the total harmonic distortion of the converter input current was less than 1.2%. Fig. 9 depicts compensation of a typical lagging power factor while maintaining constant active power flow to the converter.
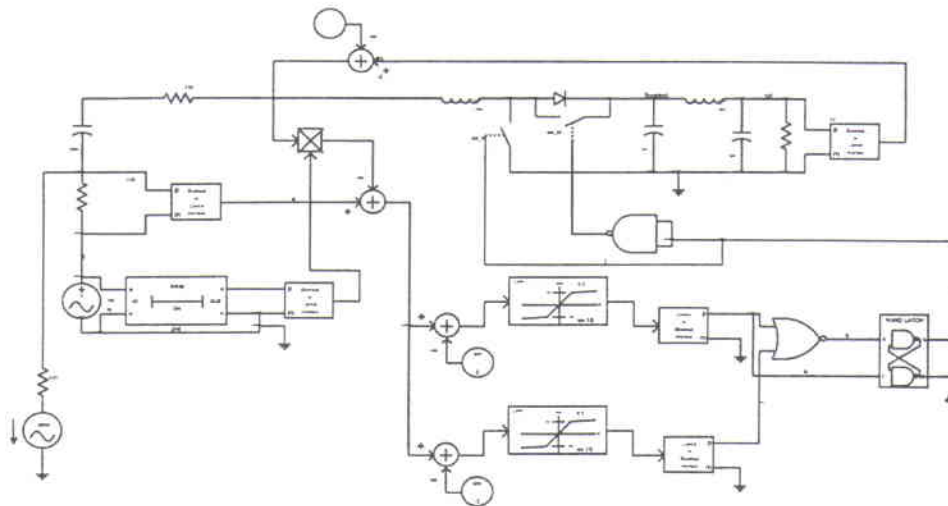
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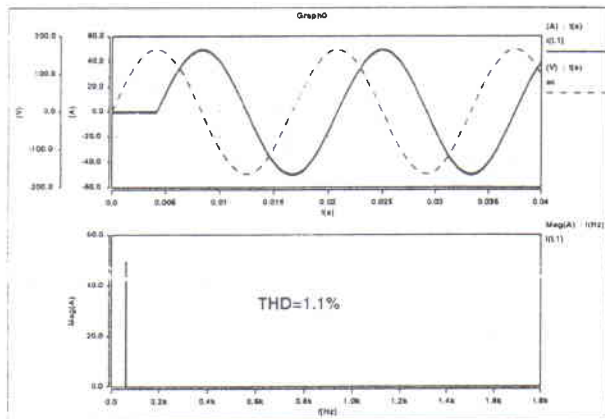Fig. 4. Saber simulation schematic for the proposed compensation system.

Fig. 6. Operation of the PFC at $\phi = 90°$. Top graph: current i_C (solid line) and mains voltage (dashed line). Bottom graph: THD of current i_C.

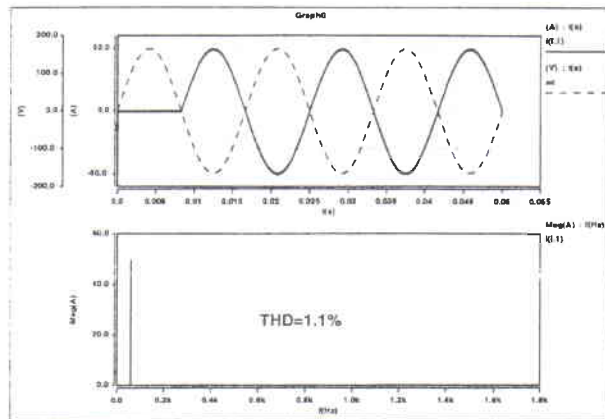
Fig. 7. Operation of the PFC at $\phi = 180°$. Top graph: current i_C (solid line) and mains voltage (dashed line). Bottom graph: THD of current i_C.

V. CONCLUSIONS

A new bidirectional adjustable-power-factor rectifier/inverter is proposed. It uses a bidirectional dc/dc converter and a bias capacitor in series with the ac voltage source. A need for a bridge diode rectifier is eliminated. A boost converter is employed as the power stage and IGBTs with antiparallel diodes act as power switches. The new topology was validated at a medium power level by Saber simulations. This paper focused on the capability of the converter to compensate reactive power of other loads. Additional advantages of this topology include: (a) removal of the diode bridge eliminates crossover distortions that are inevitable in a conventional Active Power Factor Correction (APFC) circuit with diode rectification bridge at its front end; (b) at any instance of time only one semiconductor device conducts (as opposed to three or two in conventional rectifiers), which results in higher efficiency. The disadvantages include a need for a large bias capacitor and oversized rating of the converter.

Since the converter has bidirectional power flow capability, the roles of source and load may be interchanged, resulting in an inverter. Two possible application are: 1. UPS system in which the same power-stage hardware will operate either as a High Quality battery charger or as an inverter. The operation mode will be selected by the control signal solely. 2. A solar power system with ac line backup such as in a solar powered house. This kind of a converter might serve in an energy management system to transfer power from solar arrays and batteries to ac loads or charge the batteries from ac line. With a proper control, the dc/dc part of the converter may accomplish the maximum power point tracking (MPPT) as well.
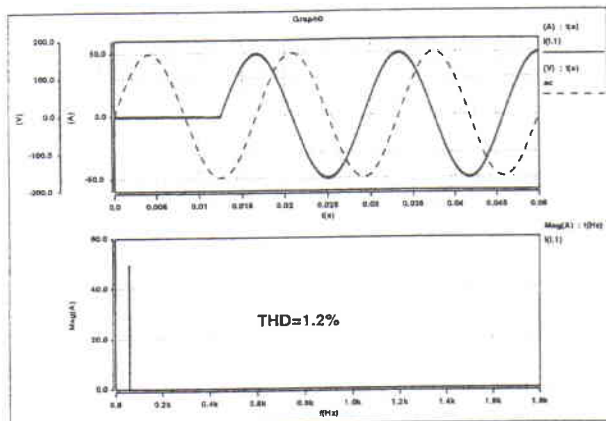
Fig. 8. Operation of the PFC at $\phi = 270°$. Top graph: current i_C (solid line) and mains voltage (dashed line). Bottom graph: THD of current i_C.
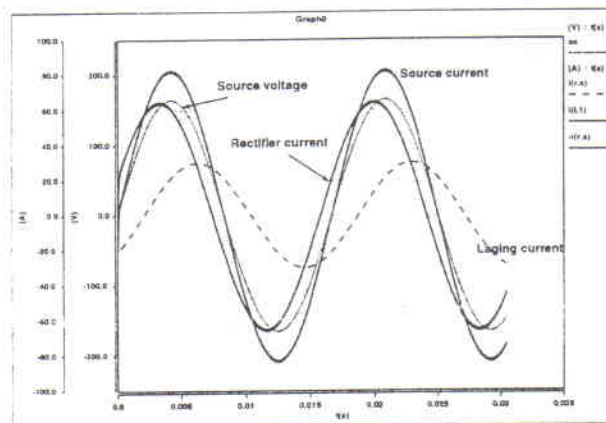

Fig. 9. Power factor compensation with constant active power at the converter output.

ACKNOWLEDGMENT

REFERENCES

[1] M. Rastogi, N. Mohan, and A.-A. Edris, "Filtering of harmonic currents and damping of resonances in power systems with a hybrid-active filter," *Proceedings of the IEEE APEC'95*, pp. 984-989.

[2] M. Rastogi, N. Mohan, and A.-A. Edris, "Hybrid active filtering of harmonic currents in power systems," *IEEE Trans. Power Delivery*, vol. 10, no. 4, Oct. 1995.

[3] J. T. Boys and A. W. Green, "Current-forced single-phase reversible rectifier," *IEE Proceedings, Pt. B*, Vol. 136, No. 5, pp. 205-211, Sep. 1989.

[4] Z. Lai and K. M. Smedley, "A family of continuous-conduction-mode power-factor-correction controllers based on the general pulse width modulator," *IEEE Trans. on Power Electron.*, vol. 13, no. 3, pp. 501-510, May 1998.

[5] S. Singer, "Applications of 'loss-free resistors' in power processing circuits," in *PESC'89 Record*, vol. 2, pp. 843-846.

[6] J. C. Salmon, "Operating a three-phase diode rectifier with a low-input current distortion using a series-connected dual boost converter," *IEEE Trans. on Power Electron.*, vol. 11, no. 4, pp. 592-603, July 1996.

[7] D. Shmilovitz, D. Czarkowski, Z. Zabar, and S.-Y. Yoo, "A novel reversible boost rectifier with unity power factor," in *Proceedings of the IEEE APEC'98*, March 14-18, 1999, Dallas, TX, pp. 363-368.