DOUBLE COMPENSATED OP-AMP INTEGRATOR

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ABSTRACT

A new method is proposed to correct the phase error in the Miller integrator. The technique utilizes two well-known compensation methods together. It provides better high-frequency performance than each of them. In the method, two complex conjugate poles are almost cancelled by introducing two real zeros located near the real part of the complex conjugate poles. The proposed idea is verified by experiment.

I. INTRODUCTION

Integrator circuits are used in many applications requiring the generation and processing of analog signals. Ideally, they posses a single pole at zero frequency. However, non-idealities of the active elements of integrators can force integrator performance to deviate from its ideal response. In particular, the finite gain-bandwidth product (GBW) of the operational amplifier (op-amp) is the cause of a phase error, which is called excess-phase shift, in the integrator response. Excess-phase shift of integrators is one of the most severe problems because it limits the integration frequency bandwidth. In order to have a wideband integrator circuit, excess-phase should be cancelled by introducing zero(s), which is called compensation. Several compensation techniques have been proposed in the literature [1 – 4]. There are two typical methods of excess-phase cancellation techniques: One is to connect a resistor in series with integrating capacitor [3, 4] and the other is to connect a capacitor in parallel with the resistor of the Miller integrator [3, 4]. Both techniques assume the one-pole model of the op-amp as in the case for other techniques in the literature [1 – 4]. In this study, the two-pole model of the op-amp, which is more realistic than the one-pole model, is taken into account and both techniques are used together at the same time as an alternative compensation method for integrators. This technique so called double compensation method is indeed the combination of two well-known techniques and gives better results than each of them according to PSpice simulation results.

II. EFFECT OF FINITE GBW

Using the one-pole model of the op-amp,

$$A(s) = \frac{A_o}{1 + \dfrac{s}{\omega_0}} \tag{1}$$

transfer function of the uncompensated original integrator is found as

$$T_o(s) = -\frac{\dfrac{A_o\omega_o}{RC}}{s^2 + \left[\dfrac{1}{RC} + (1 + A_o)\omega_o\right]s + \dfrac{\omega_o}{RC}} \tag{2}$$

where A_o is the open-loop gain at dc and ω_o is the pole frequency. According to PSpice simulation results the uncompensated Miller integrator with LM741 (National Semiconductor) op-amp and with R = 1 kΩ and C = 1 nF performs its function between frequencies 1.6 kHz and 81 kHz. Here, integration frequency band is assumed to be the range where phase difference in the output voltage with respect to the input voltage is between 85º and 95º, which is a common assumption, used in the literature [2].

By connecting a resistor, R_1, in series with the integrating capacitor transfer function becomes

$$T_1(s) = -\frac{A_o\omega_o \dfrac{R_1}{(R + R_1)}\left(s + \dfrac{1}{R_1 C}\right)}{s^2 + \left\{\dfrac{1 + \omega_o[(1 + A_o)R + R_1]C}{(R + R_1)C}\right\}s + \dfrac{\omega_o}{(R + R_1)C}} \tag{3}$$

Employing the other popular method, which is to connect a capacitor, C_1, in parallel with resistor transfer function takes the similar form with the above one, i.e.,

$$T_2(s) = -\frac{A_o\omega_o \dfrac{C_1}{(C+C_1)}\left(s+\dfrac{1}{RC_1}\right)}{s^2 + \left\{\dfrac{1+\omega_o R[(1+A_o)C + C_1]}{R(C+C_1)}\right\}s + \dfrac{\omega_o}{R(C+C_1)}} \quad (4)$$

In both compensation methods the excess-phase is cancelled by the introduced zero located at the second pole frequency. Because of using the one-pole model of the op-amp, there is only a single pole to be cancelled, which is real with the selected element values. According to PSpice simulation results upper integration frequency limit (UIFL) is increased to 454 kHz for the case of connecting series resistor with R_1 = 200 Ω and to 525 kHz for the case of connecting parallel capacitor with C_1 = 200 pF using the same op-amp and basic integrator component values.

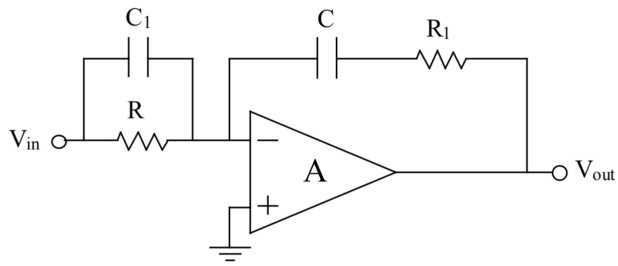

Figure 1. Proposed double compensated op-amp integrator

III. PROPOSED METHOD

Applying both compensation methods together the circuit of Figure 1 is obtained. In the analysis of this circuit the two-pole model of the op-amp,

$$A(s) = \frac{A_o}{\left(1+\dfrac{s}{\omega_0}\right)\left(1+\dfrac{s}{\omega_1}\right)} \quad (5)$$

is used. The proposed double compensation scheme aims to compensate the effect of two excess-phase shifts coming from the op-amp rather than only one as in both methods described above. Using the two-pole model of the op-amp the transfer function of the circuit of Figure 1 is derived as

$$T_3(s) = -\frac{A_o\omega_o\omega_1(1+sR_1C)(1+sRC_1)}{(s+\omega_o)(s+\omega_1)(1+sR_1C)(1+sRC_1) + s[(s+\omega_o)(s+\omega_1) + A_o\omega_o\omega_1]RC} \quad (6)$$

The first and second pole frequencies of the open-loop gain of LM741 are given as ω_o = 31.4 rad/sec (f_o = 5 Hz) and ω_1 = 16x10^6 rad/sec (f_1 = 2.55 MHz) in the PSpice macro model. The DC open-loop gain is specified to be A_o = 2x10^5 in the National Semiconductor's op-amps data book. Substituting these values together with compensation element values, R_1 = 100 Ω and C_1 = 100 pF, pole and zero frequencies of the transfer function of Equation (6) are found as ω_{p1} = 4.3 rad/sec, $\omega_{p2,p3}$ = (8±j5.7)x10^6 rad/sec, ω_{p4} = 1.2x10^8 rad/sec; ω_{z1} = ω_{z2} = 10x10^6 rad/sec. Notice that using two-pole model together with selected element values has yielded two complex conjugate poles. The effects of these poles are eliminated, though not completely, by the introduced two zeros which are located near the real part of the pole frequencies. In fact, for total elimination both real and imaginary parts of zeros and poles should be equal. However, complex conjugate poles having real parts greater than imaginary parts can almost be cancelled by introducing two zeros at the real part of the pole frequencies provided that real parts of the poles are greater than the imaginary parts. The first pole, ω_{p1}, of the transfer function of Equation (6) is needed for integration operation. The forth one, ω_{p4}, which is at very high frequency, limits the integration process at the upper side. PSpice simulation of this circuit with compensation elements R_1 = 100 Ω and C_1 = 100 pF results in integration between frequencies 1.6 kHz and 600 kHz. Therefore, this method provides wider bandwidth than preceding two ones as expected since the two-pole model of the op-amp is assumed. Figure 2 shows the PSpice simulation results. In Table 1, UIFLs of uncompensated integrator and compensated integrators using three different methods are given for comparison.

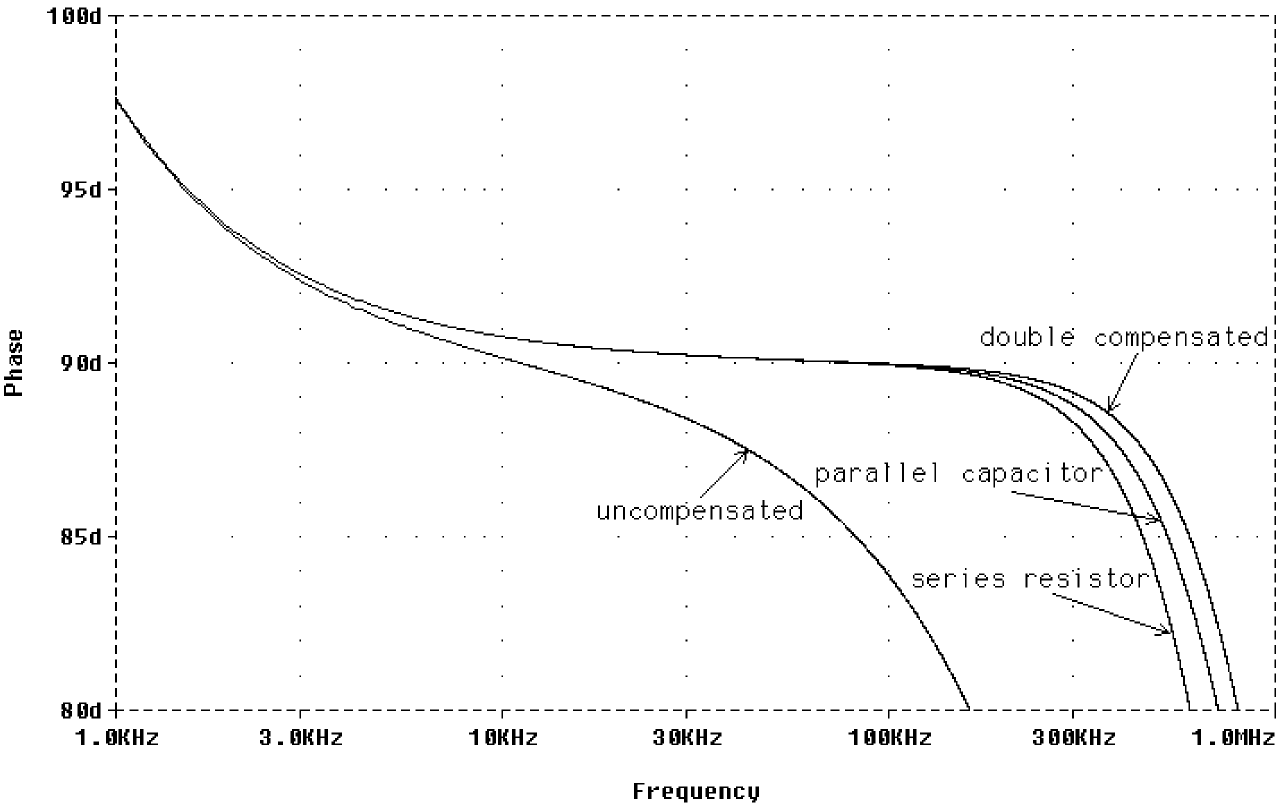

Figure 2. Phase responses of uncompensated integrator and compensated integrators using three methods

Table 1. Comparison of the compensation methods

Integrator type	R_1	C_1	UIFL (kHz)
Uncompensated	—	—	81
Series resistor	200 Ω	—	454
Parallel capacitor	—	200 pF	525
Double compensated	100 Ω	100 pF	600

IV. EXPERIMENTAL RESULTS

To demonstrate the validity of the proposed method, double compensated integrator modified by adding a feedback resistor of R_f = 100 kΩ was realized and tested in the laboratory. As the input, a square wave voltage with a frequency of 600 kHz was applied to the circuit. The output voltage was measured to be a triangular waveform as shown in Figure 3.

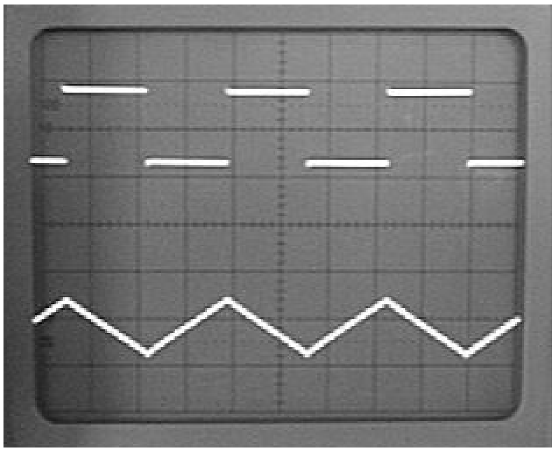

Figure 3. Input and output voltage waveforms of the realized circuit (Volts/Div = 1 V, Time/Div = 0.5 μs)

V. CONCLUSION

In this study, a novel compensation method for op-amp integrators is presented. The method is in fact the combination of two very popular methods that are connecting a resistor in series with the integrating capacitor and that connecting a capacitor in parallel with the resistor. Double compensated integrator utilizes both methods together. In contrast to most of the techniques reported in the literature, in the analysis of the proposed circuit the two-pole model of the op-amp is employed. Transfer function of double compensated integrator has two complex conjugate poles, which limit the integration bandwidth. In order to have a wideband integrator circuit, these poles are almost cancelled by introducing two real zeros near the frequency of the real part of the pole frequencies. Using the proposed circuit UIFL is raised to 600 kHz from 81 kHz. According to PSpice simulation results, double compensated integrator has wider bandwidth than the integrators that use only one compensation element. Double compensated integrator was realized and tested in the laboratory. Experimental and simulation results have confirmed the theoretical analysis of the proposed circuit.

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