STATISTICAL INVESTIGATION OF HOT-CARRIER DEGRADATION AND LIFETIME PREDICTION OF P-MOS TRANSISTORS

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ABSTRACT

In this paper the degradation in the drain current and threshold voltage of the P-MOS transistors are observed by operating the device under voltage stress conditions. Using the observartion results the effect of hot-carriers was investigated statistically and a new statistical method for modeling was proposed to be an alternative to those given in the literature. The linear regression method is used to estimate the Power, Weibull and Logarithmic parameters and the correlation coefficient is used to confirm the results. The observed and the estimated values of the degradation are compared with each other.

1. INTRODUCTION

Parallel to advances in microelectronics, computer and space technologies, the device dimensions get smaller; as a result, hot-carrier effect, lifetime prediction and reliability become more important concepts for MOS transistors.

Several works have been performed on hot-carrier effect which is one of the most important factors that influences the reliability of the MOS structures [1-19].

In most of the reliablity studies on the modelling of hot-carrier effect available in the literature, models based on physical properties have been proposed [1-8, 19]. But, difficulties in preparation of pyhsical model, loosing the actuality within the advances in the technology and too long simulation times seem to be the disadvantages of these models.

To overcome these disadvantages of the physical models, a statistical method that is based on the observation results, independent from the technology and exhibits short simulation times and high accuracy has been introduced in this work. Starting from experimental results of Siemens AG., Muenchen, Germany [19], the effect of hot-carriers on the drain current and threshold voltage of P-MOS transistors was investigated statistically and a statistical model was proposed to be an alternative to those available in the literature. The time-dependent statements of degradation was obtained by using three different statistical methods.

2. P-MOS DEGRADATION

P-MOS degradation occurs only if electrons trap in the gate oxide due to the impact ionization by hot-holes [1-9]. This is known as drain avalanche hot carrier mechanism and is shown in Figure-1. When the P-MOS transistor is operating in the saturation region, holes move from the source to drain and are accelerated by the high electric field at the drain end of the channel. If a hole has energy of at least 1.5eV then it can be concluded with impact ionization. After an impact ionization the arise of the new hole is moving to the drain, as the other holes, and it increases the drain current (I_D) a small amount. Most of the new electrons, after impact ionization, move to the substrate, forming the substrate current (I_B). But some of these electrons, if they have an energy at least of 3.1eV and the right direction, they surmount the Si-SiO_2 potential barrier and are injected into the gate oxide. The electric field strength direction, in the gate oxide above the depletion region, causes the electron to accelerate to the gate. Most of the electrons in the gate oxide reach the gate and from the gate current (I_G) which is very corresponding to the drain current (I_D). But the existing traps in the oxide can capture some of the electrons and these captured electrons behave like fixed negative charges. Electrons that injected into the gate oxide can damage the Si-SiO_2 interface. These interface defects are partly filled by the holes, in the non-saturation operation. Therefore, this degradation effect on a MOSFET will be ignored. The fixed negative charges of the captured electrons cause an increase in the drain current in all region of

operation. However, the largest degradation will be in saturation operation. For the short channel MOSFETs the threshold voltage (V_{th}) will also change to the lower values.

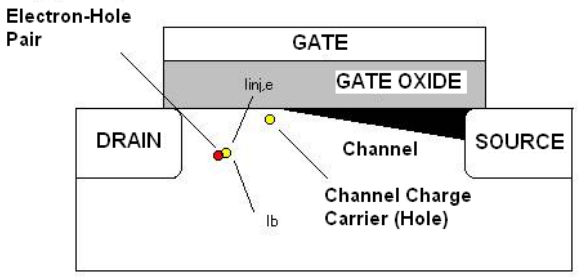

Figure-1 : Hot-carrier formation mechanism of P-MOS transistors

3. STATISTICAL METHODS

This study was performed for two different transistors produced with the same technology but with different channel lengths. Process parameters of the used transistors are given as t_{ox}=20nm, x_j=400nm, the dimensions are W=10µm, L=1.5µm and L=3µm. Stress voltage was applied to the transistors for a duration of 16 hours. Statistical methods are applied and investigated by using variation of drain currents and threshold voltages with time which are obtained as a results of applied stress voltage (V_D=0.5V, V_D=2.5V, V_G=1.5V, V_G=2V and V_G=2.5V).
The investigated methods are;

- Power method
- Weibull method
- Logarthmic method

Calculations are based on linear regration method for all of the three approaches and least squares methods have been used [14-17]. So, calculations were performed by using MATLAB program.

Exponential Distribution With Least Squares Method

$$y = Ae^{Bx}$$

$$a = \frac{\sum_{i=1}^{n} \ln y_i \sum_{i=1}^{n} X_i^{\,2} - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} x_i \ln y_i}{n\sum_{i=1}^{n} x_i^{\,2} - (\sum_{i=1}^{n} x_i)^2}$$

$$b = \frac{n\sum_{i=1}^{n} x_i \ln y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n} x_i^{\,2} - (\sum_{i=1}^{n} x_i)^2}$$

$B \equiv b$ and $A \equiv \exp(a)$.

Logarithmic Distribution With Least Square Method

$$y = a + b \ln x$$

$$b = \frac{n\sum_{i=1}^{n} (y_i \ln x_i) - -\sum_{i=1}^{n} y_i \sum_{i=1}^{n} \ln x_i}{n\sum_{i=1}^{n} (\ln x_i)^2 - (\sum_{i=1}^{n} \ln x_i)^2}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} (\ln x_i)}{n}$$

Power Distribution With Least Square Method

$$y = Ax^B$$

$$b = \frac{n\sum_{i=1}^{n} (\ln x_i \ln y_i) - \sum_{i=1}^{n} (\ln x)\sum_{i=1}^{n} (\ln y_i)}{n\sum_{i=1}^{n} (\ln x_i)^2 - (\sum_{i=1}^{n} \ln x_i)^2}$$

$$a = \frac{\sum_{i=1}^{n} (\ln y_i) - b\sum_{i=1}^{n} (\ln x_i)}{n}$$

$B \equiv b$ and $A \equiv e^a$.

4. RESULTS AND DISCUSSIONS

It can be seen from experimental results, that the drain current and the threshold voltage of P-MOS transistors increases with time. On the other hand, from a previous study [20] it can be easily observed that the drain current and the threshold voltage of N-MOS transistors decreases with time. For L=1.5µ the change in the drain current is approximately %4 for P-MOS while it is %0.8 for N-MOS. It seems that P-MOS transistors are affected more from the hot-carriers. The functions, obtained by using investigated methods, that give the percent changes in drain currents and threshold voltages are given in Table-1. The function coefficients obtained of three methods for different channel lengths can be seen in Table-2 and Table-3.

Table-1: Obtained functions of investigated methods

Investigated method	Obtained functions
Power	% $I_D(t)$= a .t^b % $V_{TH}(t)$= a .t^b
Logarithmic	% $I_D(t)$= a+b.ln(t) % $V_{TH}(t)$= a+b.ln(t)
Weibull	% $I_D(t)$= 1-exp[-$(t/a)^b$] % $V_{TH}(t)$= 1-exp[-$(t/a)^b$]

Table-2: Obtained function coefficients of P-MOS transistors for different methods for L=1.5µ

	Power	Logarithmic	Weibull
$I_D(V_D=0.5)$	a=3,158 b=0,121	a=3,036 b=0,583	a=270 b=0,174
$I_D(V_D=2.5)$	a=1,37 b=0,156	a=1,261 b=0,370	a=400052 b=0,180
$I_D(V_G=1.5)$	a=3,264 b=0,156	a=3,005 b=0,883	a=42 b=0,281
$I_D(V_G=2)$	a=1,662 b=0,156	a=1,53 b=0,449	a=8318 b=0,190
$I_D(V_G=2.5)$	a=1,513 b=0,156	a=1,393 b=0,409	a=17052 b=0,187
V_{TH}	a=0,099 b=0,141	a=0,093 b=0,023	a=293459 b=0,146

Table-3: Obtained function coefficients of P-MOS transistors for different methods for L=3µ

	Power	Logarithmic	Weibull
$I_D(V_G=1.5)$	a=4,002 b=0,156	a=3,683 b=1,83	a=42,58 b=0,28146
$I_D(V_G=2)$	a=1,202 b=0,156	a=1,106 b=0,3252	a=8318,56 b=0,19055
$I_D(V_G=2.5)$	a=0,722 b=0,156	a=0,6648 b=0,1954	a=17052,06 b=0,18707

Calculated results are compared with experimental results. It has been observed that the loarithic method seems to be the best statistical method that characterizes the measurement results, The characterization results using logarithmic method are given with experimental results in Figures 1-2. It seems from the figures that there is a good agreement between the experimental results and calculated values. To show the similarity between the measured and calculated values, correlation coefficients were calculated and very high correlation coefficients were obtained. Results obtained can be seen in Table-4. Morever, error calculations are achieved with RMS method and the results are given in Table-5. It can be easily observed that the error values are very low. With respect to graphics, correlation coefficients and RMS errors, the methods are classified from the best to worst as Logarithmic, Power ann Power methods respectively.

Table-4: Obtained correlation coefficient for P-MOS

	Logarithmic	Power	Weibull
Id (Subthreshold)	0,998482	0,990399	0,997737
Id (Inversion)	0,997117	0,988502	0,992571
Vth	0,998128	0,952594	0,9587

Table-5: Obtained RMS error for P-MOS

	Log	Power	Weibull
Id (Subthreshold)	0,03111	0,07891	0,04356
Id (Inversion)	0,02728	0,05528	0,04657
Vth	0,01377	0,08093	0,08590

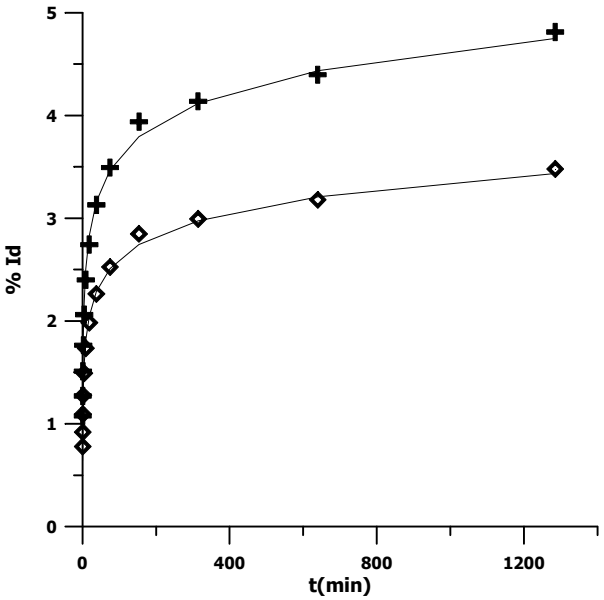

Figure-2: Measured L=3µm(✚) ,L=1.5µm (◆), and calculated (—) % I_d variations with Logarithmic method for different channel-lengths

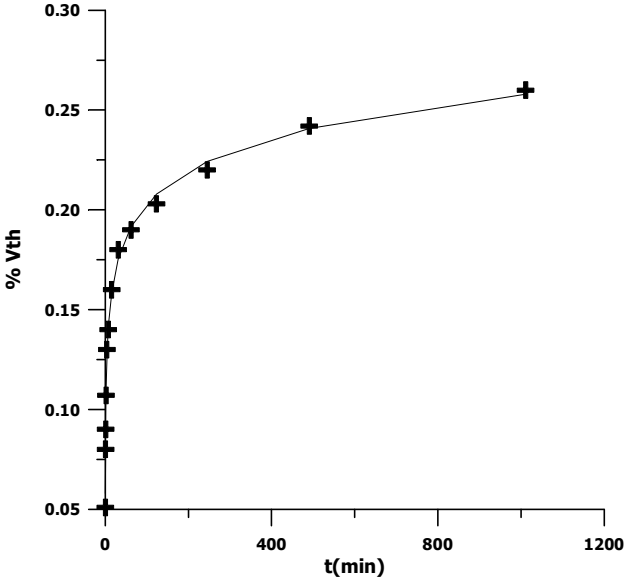

Figure-3: Measured L=1.5µm(✚) ,and calculated (—) % V_{TH} with Logarithmic method

5. APPLICATION EXAMPLE

In this section, SPICE simulation of a CMOS inverter was performed to demonstrate how the proposed method can be applied to a circuit example and to show the practicality of the method. BSIM3 MOSFET

model paramters which are used often in simulations of nowaday were used in simulations.
By using the easy CMOS stucture of Figure 4, circuit simulations were performed. Supply voltage of the circuit is chosen as V_{DD}=5V, dimensions for NMOS are W=10µ, L=3µ and dimensions for PMOS transistors are W=10µ, L=1.5µ.

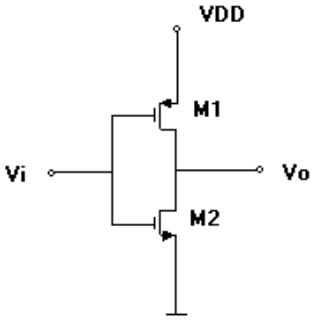

Figure-4: CMOS inverter circuit

SPICE simulation results for the change in the DC transistor characteristics of the circuit before stress and after stress are seen in Figure-5. In CMOS inverters the change of the current and threshold voltage of the transistors has an important effect on the value of inverting voltage of the circuit. Inverting voltage of the inverter was determined as V_I=2,41V and V_O=2,81V before the stress. It was observed that the value of the inverting point of the voltage transition characteristic shifted to V_I=2,41V and V_O=2,51V after a stress of 18 hours. The transfer characteristic of the inverter without considering the degradation effect caused by P-MOS transistor is given in Figure-6, assuming that the characteristic is influenced only by NMOS transistor. Before stress and after stress values of the inverter for Vı=2,41V were obtained as Vo=2,81V and Vo=2,75V respectively. As it is seen that the output characteristic of the circuit depends mostly on the change of the drain current of the PMOS. The chage of the inverting voltage value with time can be seen in Figure-7.

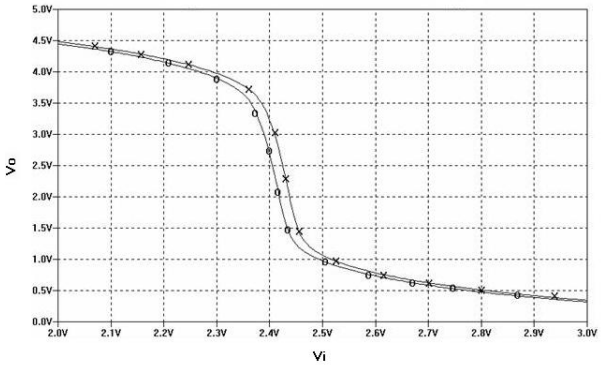

Figure-5: Before stress (x) and after stress (o) voltage transfer characteristic of the CMOS inverter

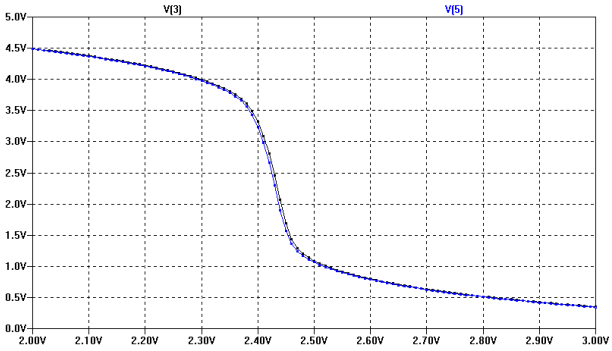

Figure-6: Before stress (x) and after stress (o) voltage transition characteristic without PMOS effect of the CMOS inverter

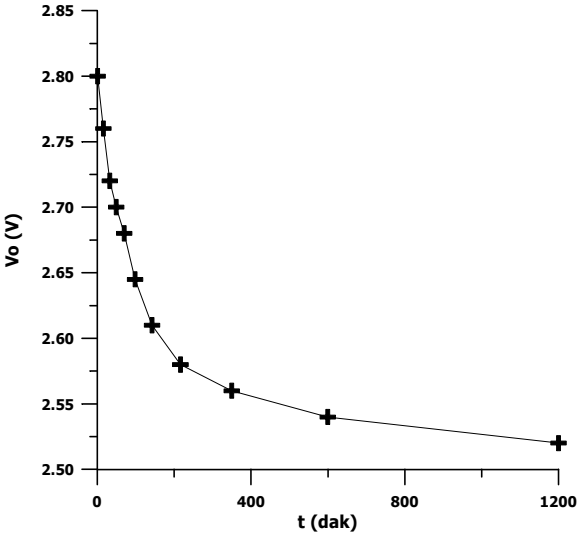

Figure-7: The change of the inverting voltage of the CMOS inverter with time

6. LIFE TIME PREDICTION

Lifetime prediction for P-MOS transistors has been performed by using the criteria given in literature [18]. It can be reached easily to a % 10 lifetime criteria of hot-carriers in DC stress application without more time than 10 years. 1 year in static conditions show 10 years in real operating condition point in analog application.
Life time prediction calculations for P-MOS were performed with respect to logarithmic method by using the functions at the proposed methods and %10 drain current criteria which is given in the literature [18]. Lifetime prediction results obtained by calculations for different operating conditions can be seen in Table-6.
Similarly, obtaining a function for the change of the output characteristic of the CMOS inverter with lifetime prediction was calculated and given in Table-7.

Table-6: P-MOS Calculated prediction lifetime for different channel length

	P-MOS Predicted lifetime (s)	
Channel length (μm)	Subthreshold region	Inversion region
L=1.5	$1{,}3x10^{5}$	$2{,}86x10^{8}$
L=3	$2{,}4x10^{6}$	$3{,}66x10^{10}$

Table-7: Calculated prediction lifetime for CMOS inverter

	Predicted lifetime(s)
CMOS inverter	$9{,}1x10^{4}$

7. CONCLUSION

The effect of hot-carriers on the drain current and threshold voltage of P-MOS transistors was investigated statistically and a method was proposed to be an alternative to those available in the literature.

Considering the correlation coefficients of the investigated methods, we see that the logarithmic method is the nearest method to 1 with 0.998. And considering the RMS errors, we see that the logarithmic method has the least error with 0.03. From this results we can say that the logarithmic method is the best method for the explanation of the change in the data. Because the proposed method is based on the measurement results and it is independent from the technology, it can be applied to P-MOS transistors which has different dimensions easily.

By using this proposed method, percentage changes in drain current which occur as a result of degradation at any time t, and threshold voltage can be find and used for the lifetime prediction of the transistor.

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