A New Reconfigurable Filter Structure Employing CDTA For Positioning Systems

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Abstract

Current differencing transconductance amplifier (CDTA) is a very useful alternative building block of current mode operational amplifiers. The analog filter types designed with CDTAs can be implemented by using only capacitors. A new reconfigurable filter employing CDTAs structure for analog signal processing is proposed in this paper. The filter structure consists of CDTAs and only two capacitors as passive element. The proposed filter structure is a part of different positioning protocols to implement on the same chip. The filter is designed with AMS 0.18µm technology. The filter performance is tested and verified by simulations with Cadence environment.

Keywords—cognitive radio, frequency agile filter, CDTA, reconfigurable filter structure, software defined radio

1. Introduction

The telecommunication is widely used in all areas of society. The basis of the communication has two essential parts as analog and digital. Although digital signal processing emerges on analog counterpart, analog signal processing is an indispensable part of the telecommunication. For example, analog filtering is one of the most important unavoidable function of transciever architectures. Nowadays, the new telecommunication technique has increased the importance of reconfigurable filters to realize more flexible transmitter and receiver blocks [1, 2].

The reconfigurable filter called as frequency agile filter is one of the background circuit of the cognitive radio, software defined radio and etc [1-3]. The frequency agile filter allows to sense different protocols with only one circuit. Such a circuit can be a signal processing part of different positioning systems bands (GPS, GLONASS, Beidou, GNSS and Galileo) to process different positioning system protocols in the same circuit [4].

In recent three decade, the research about current-mode approach has been investigated in detail. Current mode circuits have some superior advantages compared to the voltage-mode circuits. Wide bandwidth, wide dynamic range and simple circuitry with lover voltage supplies are some advantages of current mode circuits [5].

Current differencing transconductance amplifier (CDTA) is one of the useful current-mode integrated building blocks. CDTA can be considerable as different version of current mode operational amplifier [6]. CDTA consists of two input terminal, one intermediate terminal and two output terminals. The structure of CDTAs is very suitable to implement the frequency agile filter by the aid of output stage transconductance g_m.

In this study, the biquadratic filter designed those in [7] is improved as a frequency agile filter to support different GPS protocols. The feedback is taken from the low pass output of the biquadratic filter to the input by passing through another CDTA. The configurability is supported by the different g_m values of the feedback CDTAs. The current study can be considered as alternative topology given in [5, 6] and its possible practical application to support multiple global positioning systems (GPS). The output stage gm of the CDTA The designed frequency agile filter behaviors are analyzed by the simulations.

2. CDTA CMOS structure and main characteristics

CDTA (Current Differencing Transconductance Amplifier) is proposed by D. Biolek in 2003 [6]. The input stage of the CDTA consists of current differencing unit. The output stage of CDTA consists of floating current source which is the most practical version of operational transconductance amplifier (OTA). CDTA has two low input impedances and three high output impedance terminals. Two of the output terminals are obtained by transmitting the current differencing unit output from floating current source which has gain defined as g_m. The CDTA has significant facility to implement current mode active filter synthesis by the aid of g_m. The current differencing unit used at the input stage of the CDTA has very stable current dynamic range. The stability of the current differencing unit is maintained for low biasing currents as 10µA. The CMOS structure used for current differencing unit has also low input impedance levels. The current differencing unit input impedance levels are very important for current mode analog signal processing because of the signals in current mode application transferred in terms of currents.

The floating current source proposed by Arbel and Goldminz has only four transistors except biasing current transistors [8]. The improved version of the floating current source has high output impedance those in [9]. The improved version of the floating current source is used at the output stage of the CDTA.

The symbol and the schematic view of the CDTA is given in the Fig. 1, 2, respectively. CDTA defining equation matrix and its basic operation formulas are given in Eq. 1.

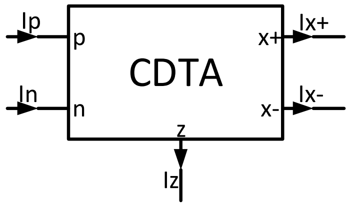

Fig. 1. The schematic view of the CDTA

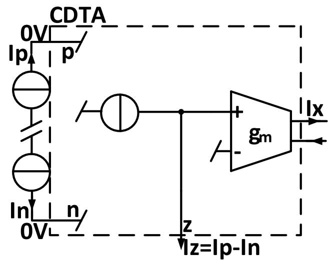

Fig. 2. The block diagram of the CDTA

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_{x\pm} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \end{pmatrix} \quad (1)$$

The CMOS structure of the CDTA is given in Fig. 3. The current differencing unit stage of the CDTA consists of the M1-M12 transistors. The floating current source of the CDTA consists of M13-20 transistors. The Mb1-Mb9 transistors are used for biasing the current differencing unit and the improved floating current source. The biasing current is generated from bootstrap current reference circuit. The biasing transistors reflects the biasing current by unity ratio. The trans-conductance of the improved floating current source can be modified by changing the ratios of Mb6-Mb9 transistors.

The biasing voltages are selects as V_{b1}=600mV, V_{b2}=-600mV, V_{b3}=-300mV and V_{b4}=300mV.

The transistor sizes of the CDTA given in Fig. 3 are given in Table I. The performance characteristics of the CDTA are given in Table II. The dc current dynamic change at Z terminal is observed between ±100µA. The input impedance characteristics of the CDTA given in Table II are observed 391Ω for P input terminal and 198Ω for N input terminal. The input impedances are good as possible for the current mode reconfigurable filter application.

The Z terminal output impedance is specified as 297kΩ. The transconductance value (g_m) of the improved floating current source structure is obtained as 443µA/V for 60µA biasing current. The X terminals output impedances are found 18.4MΩ. These X terminal impedances have a large value compared to the classical floating current source CMOS structure [8]. The X terminals output resistances are very uselful to achieve high attenuation and high quality factor in despite of low bandwidth of the CDTA. The f_{-3dB} cut-off-frequency for I_z/I_p and I_z/I_n are measured as 925MHz, 524MHz, respectively.

Table 1. The size of the transistors

Transistors	Value
M_1, M_2, M_3, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}	72u/0.36u
M_4, M_5	144u/0.36u
M_{b3}, M_{b4}, M_{b7}, M_{b8}	72u/0.36u
M_{b1}, M_{b2}, M_{b5}, M_{b6}, M_{b9}	24u/0.36u
M_{13}, M_{14}	36u/0.36u
M_{15}, M_{16}	12u/0.36u
M_{17}, M_{18}	54u/0.36u
M_{19}, M_{20}	18u/0.36u

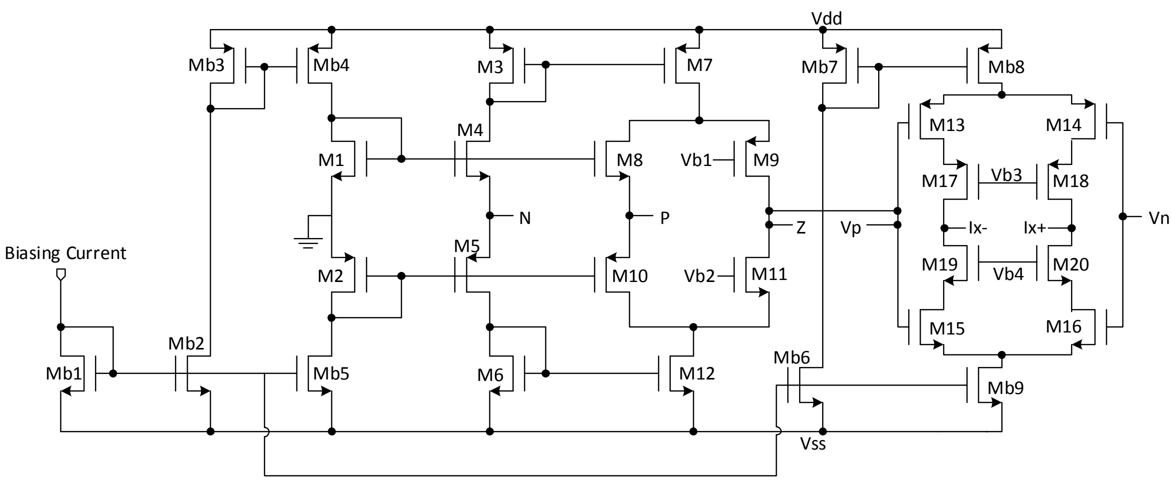

Fig. 3. CMOS structure of the CDTA

Table 2. The performance characteristics of CDTA

Results	Values
Supply voltage	±0.9 V
Power dissipation	3.888 mW
Z terminal current dynamic range	-100µA ≤ Iz ≤ 100µA
f_{-3dB} frequency for Iz/In	524MHz
f_{-3dB} frequency for Iz/Ip	925MHz
P terminal input impedance	391.237Ω
N terminal input impedance	198.644Ω
Z terminal output impedance	242.677kΩ
X± terminal output impedances	18.4MΩ

3. Reconfigurable Filter Structure

The general class-1 reconfigurable filter structure is shown in Fig. 4 [5]. The frequency agile filter structure can be realized by using a general second order filter which has low pass and band pass output. The low pass output can be directly applied to the input by passing through a gain stage given an in Fig. 4. The current differencing transconductance amplifier g_m is very useful to obtain the gain of A.

Fig. 5 shows CDTA based biquadratic filter structure. This structure is multi output and multifunctional filter. In other words, the biquadratic filter has band pass, high pass and low pass filter sections.

The band pass filter transfer function of the biquadratic filter structure is given in Eq. 2. The center frequency and quality factor of the biquadratic filter structure are given in Eq. 3, 4, respectively. This filter capacitance values C1=C2=1pF are determined for appropriate center frequency range of positioning systems protocols.

The sensitivity analyses of the biquadratic filter with respect to active and passive components yield the following Eq. 5, 6, respectively.

$$\frac{I_{BP}}{I_{IN}} = \frac{s g_{m1} C_2}{s^2 C_1 C_2 + s g_{m1} C_2 + g_{m1} g_{m2}} \tag{2}$$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{3}$$

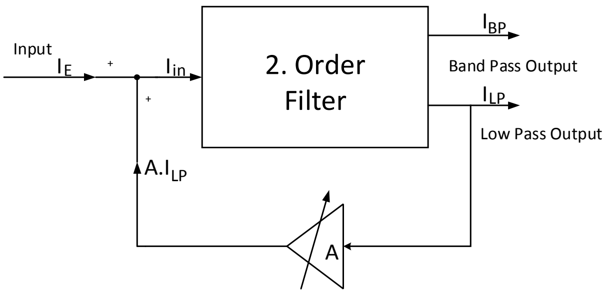

Fig. 4. Second order current mode reconfigurable filter [5]

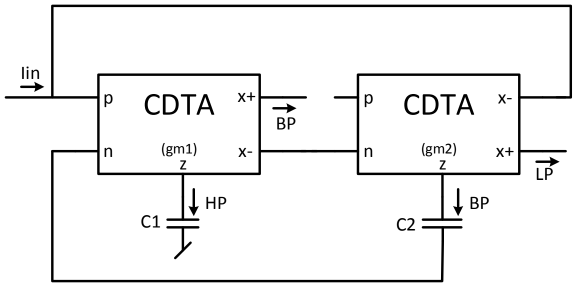

Fig. 5. CDTA based biquadratic filter structure [9]

$$Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}} \tag{4}$$

$$S_{g_{m1}}^{\omega_0} = S_{g2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = 0.5 \tag{5}$$

$$S_{g_{m1}}^{Q} = S_{g_{m2}}^{Q} = S_{C_1}^{Q} = -S_{C_2}^{Q} = 0.5 \tag{6}$$

The gain gm_fb of the feedback CDTA's effects also the quality factor of the reconfigurable filter output. The x+'s band pass section is used for the simulations. The output of the frequency agile filter is given in Fig. 6.

The proposed frequency agile filter structure is given in Fig. 7. The configurability is obtained by switches. All feedback CDTA's g_m is designed according to the positioning systems.

The low pass output of the proposed CDTA biquadratic filter structure is fed back with another CDTA. The improved floating current source at the output stage of CDTA has a g_m gain. The configurability of the new filter is provided by the aid of the feedback CDTA g_m as A (feedback gain given in Fig. 4) [3-4]. The new band pass function is given in Eq. 7. The center frequency, quality factor of the designed filter are changed according to the Eq. 8, 9, respectively.

The trans-conductance of CDTA's used in frequency agile filter structure are given in Fig. 8. It is obviously seen that the higher gm_fb is used to achieve higher frequencies. The total harmonic distortion according to the input current at 54.9MHz is given in Fig. 9. The designed filter harmonic distortion is less than 5% up to 100µA input current.

$$\frac{I_{BP}}{I_E} = \frac{\dfrac{C_2 g_{m1} s}{(1 - g_{m\_fb} \cdot g_{m1} \cdot g_{m2})}}{1 + \dfrac{C_2 g_{m1} s}{(1 - g_{m\_fb} \cdot g_{m1} \cdot g_{m2})} + \dfrac{C_1 C_2 s^2}{(1 - g_{m\_fb} \cdot g_{m1} g_{m2})}}$$

$$\omega_{0\_new} = \sqrt{\frac{(1 - g_{m\_fb} \cdot g_{m1} g_{m2})}{C_1 C_2}} \tag{7, 8}$$

$$Q_{new} = \sqrt{(1 - g_{m\_fb} \cdot g_{m1} \cdot g_{m2})} \sqrt{\frac{C_1 C_2}{C_2 g_{m1}}} \tag{9}$$

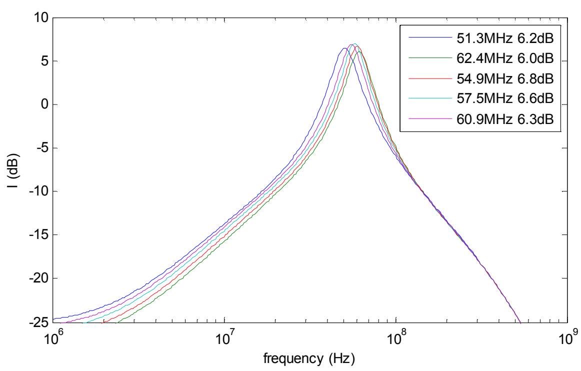

Fig. 6. The frequency agile filter output

The switches are activated one by one to achieve the desired center frequency. The feedback CDTA's Z terminal current gives the p terminal current because of the grounded n terminal. The RZ resistances are used to ensure the stable voltage drop at the Z terminal. Thus, the gm of the output stage of the CDTA directly affects the center frequency.

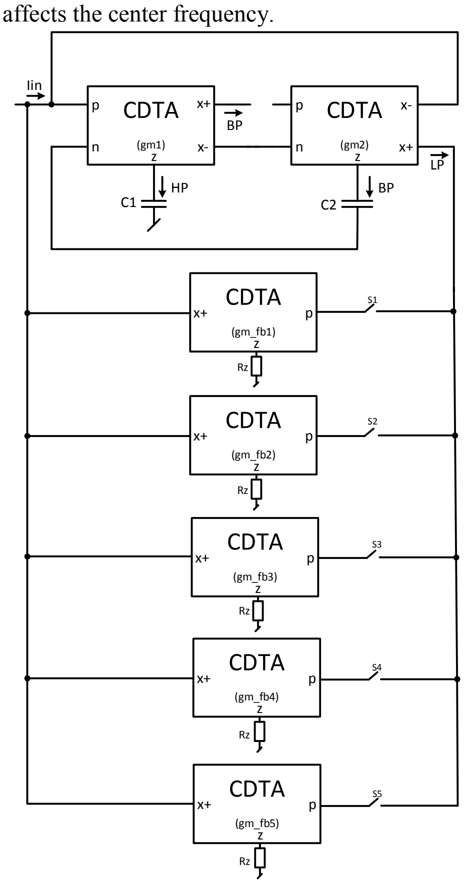

Fig. 7. The proposed reconfigurable filter structure

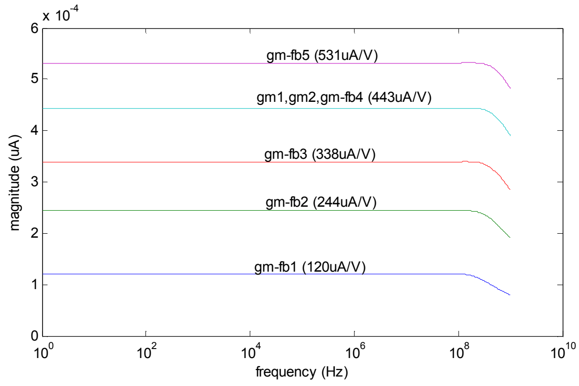

Fig. 8. The transconductance of the CDTA's

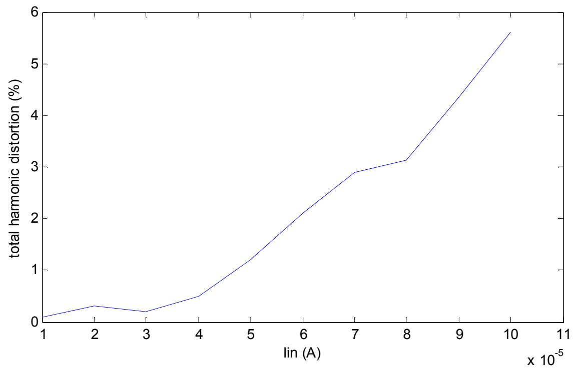

Fig. 8. The total harmonic distortion with respect to input current at 54.9MHz

4. Conclusions

A new reconfigurable filter structure improved with current differencing transconductance amplifier is proposed in this paper. The proposed filter structure is designed to detect different positioning system protocol bands (GPS, GLONASS, Beidou, GNSS and Galileo) by changing the transconductance of the feedback's CDTA with different biasing current. CDTA's CMOS structure and the reconfigurable filter performance parameters are given in the study. The simulations of the design are realized with AMS 0.18µm transistor technology in CADENCE environment.

7. References

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