Input and Output Matched SiGe RF Mixer with High Dynamic Range

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Abstract

An active mixer operating at 2.15 GHz which is based on the Gilbert Mixer topology is designed by using the transistors which are realized by using 0.25um SiGe technology. The symetrical driving circuit at the input is realized by using the CB(common base) and CE(common emitter) transistors which operate interactively. The passive capacitive voltage-series feed-forward circuit is applied to CB circuit and an almost perfect broadband matching is obtained at the input. Mixer is simulated with AWR software environment. 5V DC supply voltage is used , OIP3 of 24.7 dBm and the Conversion Gain of 3 dB is obtained for the -2.5 dBm of LO power. The noise figure of the circuit is simulated as 11.75 dB.

1. Introduction

This paper presents a mixer which is designed for to be used as the second mixer stage in a RF receiver IC. The performance requirements are specified as; 3 dB Conversion Gain, OIP3 of minimum 23 dBm and the noise figure of maximum 12dB. The mixer is consists of a modified Gilbert Cell where the input voltage –current converting stage is realized by using CB and CE stages which operate interactively to provide matching at the input. The IF output amplifying stage with reasonably high dynamic range is arranged as the combination of the inverting and non-inverting stages to provide the power doubling at the output. Gilbert Cell is the most common double balanced mixer switching topology which is used in various RF IC applications. It is quite convenient to obtain the high gain with high dynamic range and low power consumption by using this circuit [2]. The modified version of this circuit which is presented in this work eliminates the use of any passive baluns at the both ports.

The topology which is used as the balanced voltage-current converter at the input is shown at Fig. 1. The feed-forward connection from the CE to a CB stage with capacitive voltage divider is used for to provide matching at the input. This technique provides highly broadband input matching with the advantages of good linearity and less noise-figure than the other techniques[1].

At the switching transistors, a small change on the switching voltage can modulate the switching time and creates distortion on the differential current waveform.

It is shown in (1) that the flicker noise coming to output from the switching transistors is proportional to the current. $S_{1/f}$ is the power spectral density of the noise, $\propto_H$ is Hooge constant, $\propto$ and γ are constants where their values depend on the material which is used in the production.

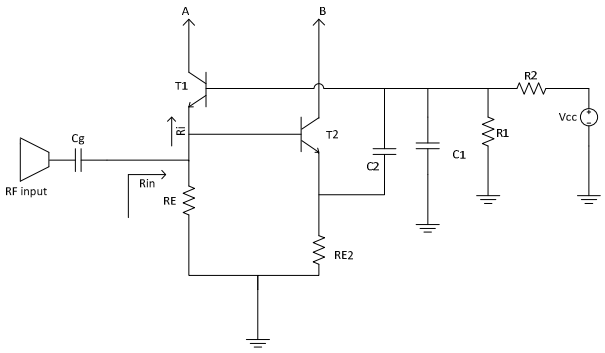

Fig. 1. Input amplifier stage of mixer circuit

$$S_{1/f} = \frac{\propto_H I^{\propto}}{f^{\gamma} N} \quad (1)$$

To reduce the flicker noise coming from the Gilbert Cell, the currents which flow through the load resistors and switching transistors is decreased by injecting a current to the connection point of Gilbert Cell through resistors [3].

2. Circuit Design

The RF input power is considered as 6dBm (4 mW) for the initial theoretical calculations,. The rms value of the RF input voltage may be calculated from (2) by taking the input impedance as 50Ω which yields as V_{RF}=0.45 V. Thus, the peak value of input voltage is readily found as 0.65 V.

$$\frac{{v_{RF}}^2}{4R_s} = P_{input} \quad (2)$$

The peak value of the input current equation with respect to the node n1 in Fig. 1. can be written as in (3) by neglecting the base current of the CB stage.

$$\frac{v_{RF,peak}}{R_{in}} = \frac{v_{RF,peak}}{R_E} + \frac{v_{RF,peak}}{R_i} = i_{in,peak} \quad (3)$$

The maximum value of the voltage variation on the node n2 is considered as slightly higher than the peak value of RF input voltage at the input node. If the DC voltage of node n2 is taken as 0.7V than the voltage of node n1 is calculated as 1.55V by adding 0.85 V of the base-emitter voltage of the transistor.

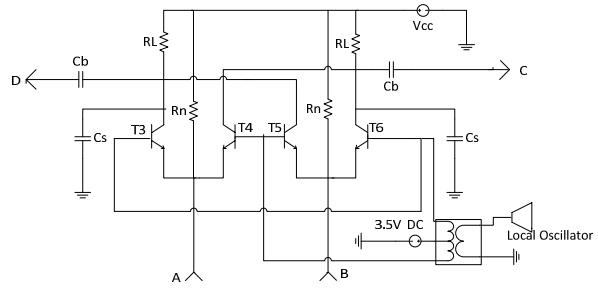

Fig. 2. The Gilbert Cell topology which is used in this work

As can be seen from (4), the maximum peak value of the input current of CB stage must equal to the emitter DC current values of the input transistors T1 and T2;

$$\frac{v_{n1}+v_{BE}}{R_E} = \frac{v_{RF,peak}}{R_i} = I_Q \qquad (4)$$

RE value is calculated as 170Ω when this equation is used in (3) and 71 Ω is obtained for the resistor Ri from (4).

The value of RE2 is also taken as 71Ω because the currents which flow through T1 and T2 must have the same value and this current value was calculated as 8mA.

The value of re value is calculated as 2.8Ω for these transistors by using the following equation:

$$r_e = \frac{1}{g_{mQ}} = \frac{V_t}{I_Q} \qquad (5)$$

Feed-forward technique with capacitive voltage divider is used to provide the input impedance matching. Because the voltage divider is realized by using the capacitors instead of resistors the effect of this stage on the noise figure is minimized. Also, dynamics of the circuit was not negatively affected due to the feed-forward.

The input current equation of the CB transistor stage can be written as follows:

$$\left(v_{in} - v_{in}\frac{C_2}{C_1+C_2}\right) g_{mQ} = v_{in}\frac{C_2}{C_1+C_2} g_{mQ} = i_i \qquad (6)$$

Since, $(\frac{v_{in}}{i_i}) = R_i = 71\ \Omega$ is found in the previous analysis (C_1/C_2) ratio is found as 22 from (6) for the perfect input match. C1=90fF is found to be the best suited value during the optimization of the capacitor values.

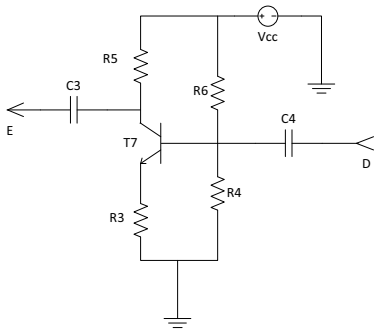

Fig. 3. Output voltage phase inverting stage.

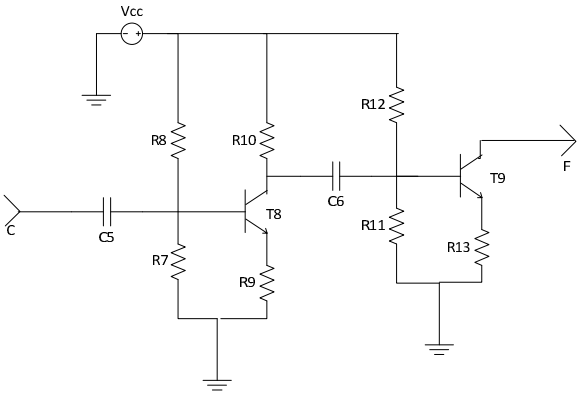

Fig. 4. Output stage without inverting.

Local oscillator voltage fluctuates over 3.5V DC value because of the bias conditions of the circuit. Since, minimum 0.1V local oscillator signal amplitude is required for the full toggling of the switching transistors the collector voltages needed to be greater than 3.6V. On the bases of this situation the load resistors of the Gilbert Cell are calculated as R_L=77 Ω.

Following the Gilbert Cell, as can be seen from Fig.3 and Fig.4, amplifying process was applied with highly dynamic, common emitter stages.

3. Noise Calculations

The noise sources of the mixer circuit can be written as:

- $\overline{v_{nRF}{}^2} = \frac{4kT}{2g_{m-upper}}$: Noise at RF due to the switching transistor.
- $\overline{v_s{}^2} = 4kTR_{source}$: Noise due to the source.
- $\overline{\iota_{n1}{}^2} = \frac{4kTg_{m-bottom}}{2}\left(\frac{R_{source}}{2R_i} - 1\right)^2 + 4kT\frac{1}{R_{E1}}\frac{R_{source}{}^2}{R_i{}^2}\frac{1}{4}$: Noise coming from amplifying stage. It consists of noise of bottom transistor and noise of RE1 resistor.

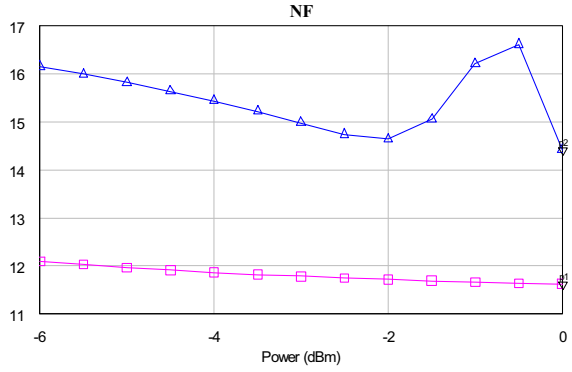

Fig. 5. Simulation result for local oscillator power level vs. noise figure graph.

- $\overline{v_{n2}{}^2} = \frac{4kT}{2g_{m-upper}}$: Noise at IF due to the switching transistor.
- $\overline{\imath_{n2}{}^2} = \frac{4kT}{R_{E2}}$: Noise coming from amplifying stage. It consists of noise of bottom transistor and noise of RE2 resistor.
- $\overline{v_{n3}{}^2} = \frac{4kT}{2g_{m-upper}}$: Noise at IF due to the switching transistor.

Noise figure is calculated from these sources with respect to (7) [4].

$$NF = 10log\frac{P_{NT,out}(\omega_{IF})}{P_{NS,out}(\omega_{IF})} \quad (7)$$

Total noise of circuit can be written as follows:

$$P_{NT,out}(\omega_{IF}) = \overline{\imath_{n1}{}^2}\frac{1}{\pi^2}\frac{g_{m-upper}{}^2R_L{}^2}{g_{m-upper}{}^2+\omega_{RF}{}^2C_P{}^2} + \overline{v_{nRF}{}^2}\frac{1}{\pi^2}\omega_{RF}{}^2C_P{}^2R_L{}^2 + \overline{\imath_{n1}{}^2}\frac{R_L}{4} + \overline{v_{n2}{}^2}\frac{\omega_{IF}{}^2C_P{}^2R_L{}^2}{4} + 4kTR_L + \overline{v_s{}^2}\frac{g_{m-upper}{}^2R_L{}^2}{g_{m-upper}{}^2+\omega_{RF}{}^2C_P{}^2}\frac{1}{\pi^2}\frac{1}{4R_i{}^2} + \overline{\imath_{n2}{}^2}\frac{1}{\pi^2}\frac{g_{m-upper}{}^2R_L{}^2}{g_{m-upper}{}^2+\omega_{RF}{}^2C_P{}^2} + \overline{v_{nRF}{}^2}\frac{1}{\pi^2}\omega_{RF}{}^2C_P{}^2R_L{}^2 + \overline{\imath_{n2}{}^2}\frac{R_L}{4} + \overline{v_{n3}{}^2}\frac{\omega_{IF}{}^2C_P{}^2R_L{}^2}{4} + 4kTR_L + \overline{v_s{}^2}\frac{g_{m-upper}{}^2R_L{}^2}{g_{m-upper}{}^2+\omega_{RF}{}^2C_P{}^2}\frac{1}{\pi^2}\frac{1}{4R_i{}^2} \quad (8)$$

The terms in the (8) is weighted bearing in mind that when all switching transistors are on, noise coming from amplifying stage is cancelled due to differential output. The noise figure of the circuit was calculated as 16.3 dB from these equations. Although current noise of the second transistor of the amplifying stage flows through capacitive voltage divider and is added to the noise of first transistor, this reducing effect was not seen from the above equations. Therefore, overall noise figure of the circuit is less than 16.3 dB.

To decrease the noise figure, it was aimed to reduce the current flows through switching transistors and their load resistors. Therefore as shown in Fig. 2., a current was injected through the resistors Rn, directly to the input branches of the Gilbert Cell. Thus the noise figure of the circuits was decreased by approximately 3dB.

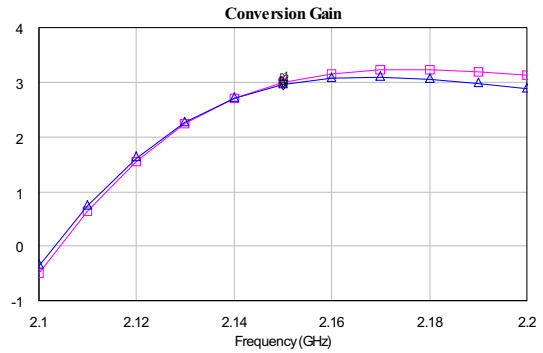

Fig. 6. Simulation result for input frequency vs. conversion gain

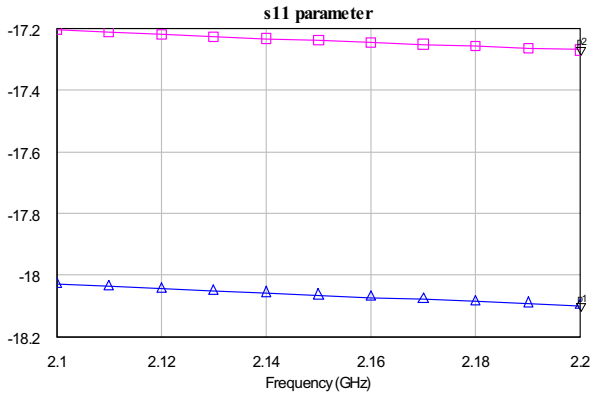

Fig. 7. Simulation result for s11 parameter

4. Simulation Results

AWR Design Environment is used for the simulation of the circuit for calculated values and then for the optimization of the performance parameters. The circuit which is used for simulation is given with Fig.9. Simulation results for noise figure, conversion gain, s11 parameter and OIP3 is given with Fig.5, Fig. 6, Fig.7 and Fig.8 respectively.

5. Conclusions

According to the simulation results the target values are obtained by optimization of calculated values. Table shows the circuit parameters for 2.15 GHz RF input and 200 MHz IF output signals. The local oscillator signal is at 2.35 GHz and it is kept at -2.5dBm power level.

Table 1. Circuit parameters

Parameter	Value (before current reduction)	Value (after current reduction)
Gain	3.0dB	3.0dB
Noise figure	15.2dB	11.75dB
Reflection from input (s_{11})	-17.24dB	-18.07dB
Output third order intercept point	4.2dB	24.7dB

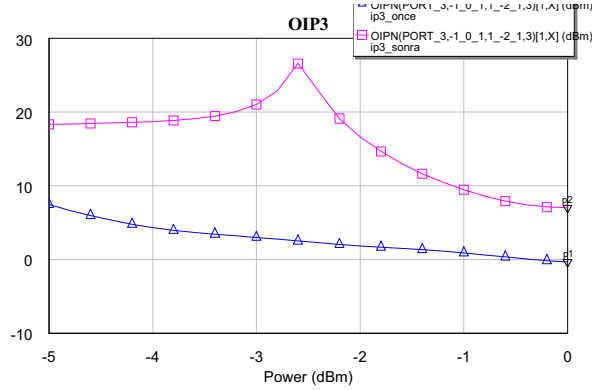

Fig. 8. Simulation result for local oscillator power level vs. OIP3

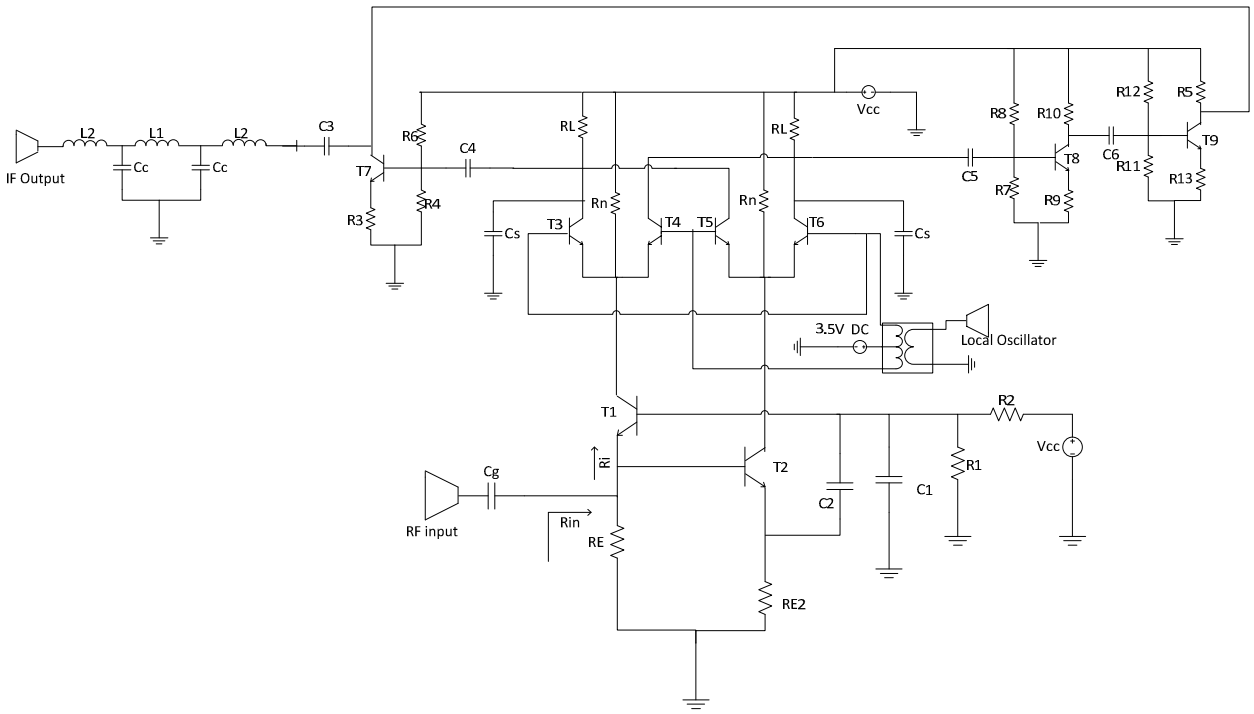

Fig. 9. The circuit used for simulations.

7. References

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[2] Gilmore, R. and Besser, L., "Practical RF Circuit Design For Modern Wireless Systems", *Artech House*, Vol. 2, *2003, p S480.*

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