On the Frequency Compensation of Some Electronic Functions Using Translinear Conveyors.

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Abstract— Integrator and differentator functions implemented from current controlled conveyors and operating either in voltage mode or in current mode will be analyzed in this paper. Various compensation methods will be investigated and the frequency response for compensated and uncompensated functions will be compared.

I. INTRODUCTION

Since they were introduced in 1970 [1], the second generation current conveyors (CCII) have led to a great number of applications in analog electronics and signal processing circuits [2,3]. Recently, taking advantage of the current controlled resistance R_x that arises from the translinear input cell of the CCIIs, the current controlled conveyors (CCCII) were introduced [4]. This give to the current conveyors high versatility and allow current conveyor applications to be extended to the domain of electronically adjustable functions.
Integrators and differentiators functions that are basic building blocks in analog electronics [5] can be directly implemented from controlled conveyors. In addition these implementations do not necessitate feedback. In this paper the basic implementations for voltage mode and current mode integrators and differentiators will be analyzed firstly. Then, the various compensation methods will be investigated and the frequency responses with compensated and uncompensated implementations will be compared.
All simulated characteristics have been determined from SPICE simulation using the MOS transistors of AMS 0.8µm CMOS fabrication process [6].

II. SECOND GENERATION CURRENT CONTROLLED CONVEYOR

II.1 Definition of the ideal CCII
The ideal second generation current conveyor given in Fig.1(a) can be described by the matrix-relation written as [4,9]:

$$\begin{pmatrix} i_Y \\ v_X \\ i_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix} \quad (1)$$

In this expression, the current transfer i_Z/i_X is equal to +1 for a positive current transfer conveyor (CCII+) and equal to -1 for a negative transfer conveyor (CCII-). The input impedances for the ideal CCII are respectively infinite on port Y and null on port X. The port Z, that is equivalent to a current generator, possesses in consequence an infinite impedance.

II.2 CMOS current controlled implemenatation
The schematic implementation of the CMOS second generation current controlled conveyor with a positive transfer from X to Z (CCCII+) is shown in Fig.1(b) [4,7]. All transistors of this class AB configuration operate in strong inversion [7,8]. The circuit uses a mixed translinear loop consisting of two NMOS (M1, M2) and two PMOS (M3, M4) transistors. The two current mirrors (M9, M10 and M11 to M13) allow the mixed loop to be dc biased by the control current I_{SS}. Assuming a low magnitude for the input current $i_X(t)$ (ie. $|i_X(t)| << I_{SS}$), the mixed loop forces the drain currents of transistors M1, M2, M3 and M4 to be equal to I_{SS} [4]. This consequently gives $V_X(t) = V_Y(t)$. The current at X is mirrored to port Z by the two complementary output mirrors (M5, M6) and (M7, M8), hence $i_X(t) = i_Z(t)$. A current controlled conveyor with negative current transfer (CCCII-) is also obtained easily, by adding two cross-coupled current mirrors to the implementation above, in order to reverse the sign of current $i_Z(t)$ [4,9].

II.3 The real conveyor and its parasitic elements
Generally the CCCII is described by the matrix-relationship shown in equation (1). But it really exhibits other parasitic impedances [12]. Indeed, between respectively each port X, Y, Z and the ground, the circuit exhibits a parallel equivalent parasitic impedance. Rx is the output resistance of the equivalent Thevenin generator seen from port X. In addition, the voltage transfer between Y and X noted $\beta(s)$ and the current transfer between X and Z noted $\alpha(s)$ exhibit dc gain values that deviate from unity as well as finite –3dB bandwidths. These transfers are generally described by the following first order functions:

$$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta} \quad (2)$$

$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha} \quad (3)$$

Fig.2 shows the general equivalent circuit that will be used to represent the behavior of the real translinear conveyors. The controlled conveyor is represented by dotted lines. It contains an ideal CCCII defined by the relation (1). The real matrix equation between the input/output ports then becomes:

$$\begin{pmatrix} i_Y \\ v_X \\ i_Z \end{pmatrix} = \begin{pmatrix} \dfrac{1}{(R_Y // C_Y)} & 0 & 0 \\ \dfrac{(R_{//X} // C_{//X})}{((R_{//X} // C_{//X}) + R_X)} & R_X & 0 \\ 0 & \alpha(s) & \dfrac{1}{(R_Z // C_Z)} \end{pmatrix} \begin{pmatrix} v_Y \\ i_X \\ v_Z \end{pmatrix} \quad (4)$$

In this way, Table 1 gives the main characteristics of the CMOS CCCII. The different simulations were obtained with SPICE simulator using the MOS transistors of AMS 0.8µm CMOS fabrication process for a bias current I_{SS}=100µA and ± 3.3V supplies.

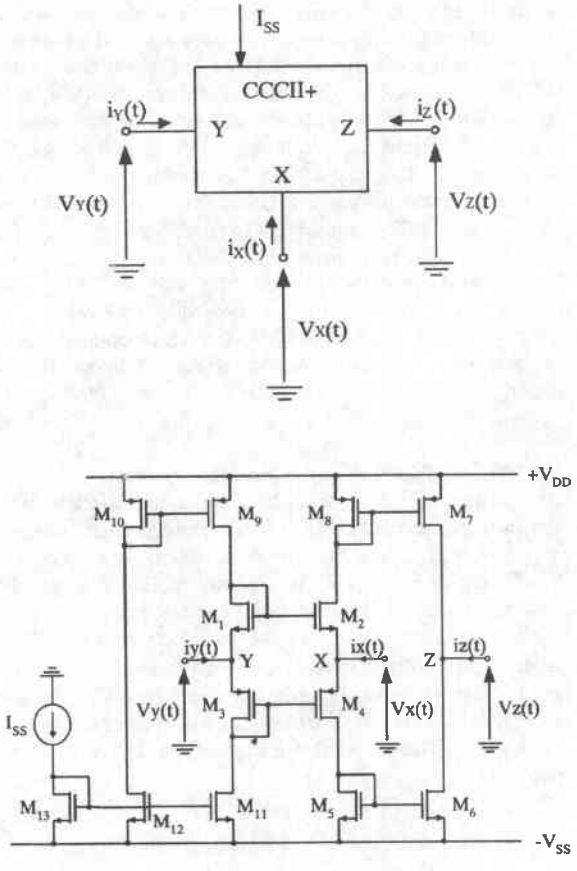


Fig.1: The translinear CMOS CCCII+.
(a) Electrical symbol.
(b) Schematic implementation.

III. INTEGRATOR FUNCTIONS

III.1 Ideal integrator

Both, voltage-mode and current-mode integrator functions will be analyzed in this section. Their real transfer characteristics, obtained from simulations with the

AC Characteristics	
α_0 = 1.02	-3dB bandwidth for α: 344 MHz
β_0 = 0.992	-3dB bandwidth for β: 456 MHz
R_Y = 168.6 KΩ	C_Y = 0.5pF
R_Z = 136.9 KΩ	C_Z = 0.07pF
R_X = 928Ω	$C_{//X}$ = 408pF
$R_{//X}$ = 102MΩ	
DC Characteristics	
Input offset current at Y	I_{yoff} = 1.21µA
Output offset voltage at X	V_{xoff} = 795µV
Output offset current at Z	I_{zoff} = -1.33µA

Table1: AC and DC characteristics of the CMOS CCCII, I_{ss} = 100µA, ± 3.3V supplies.

conditions above, will be compared to the ideal ones that would be obtained with an ideal conveyor. An ideal integrator function, $F(s) = 1/\tau s$, is characterized by an infinite low frequency gain, a -90° phase shift, and a -6dB/octave gain variation. Its time constant is $\tau = R_X C$, and the unity gain frequency for is $\omega_\tau = 1/\tau$ (see for example Fig.4).

III.2 Voltage mode integrator

Fig.3 shows the voltage mode integrator implemented from the CCCII+. In this circuit a voltage current conversion is achieved from the intrinsic resistance R_X. This conversion ratio is adjustable from I_{ss}, which allows to adjust the value of the time constant of the integrator. This circuit exhibits a high input impedance at Y. To preserve the right operating, the output voltage must be taken out at high impedance using an additional voltage buffer for example.

When all the parasitic elements of the conveyor are taken into account, the transfer function of the circuit in Fig.3 is:

$$F_v(s) = \frac{V_{out}}{V_{in}}(s) = \frac{R_Z}{R_X} \frac{\alpha_0}{1 + s/\omega_\alpha} \frac{1}{1 + R_Z(C + C_Z)s} \quad (5)$$

Where $G_0 = R_Z/R_X$, is the low frequency gain of the real integrator. $\alpha_0/(1 + s/\omega_\alpha)$, that results from the output current mirrors gives the value of the high cut off frequency $f_H = 1/2\pi\omega_\alpha$. The last term in equation(5), results from the parasitic elements at port Z of the CCCII and gives the

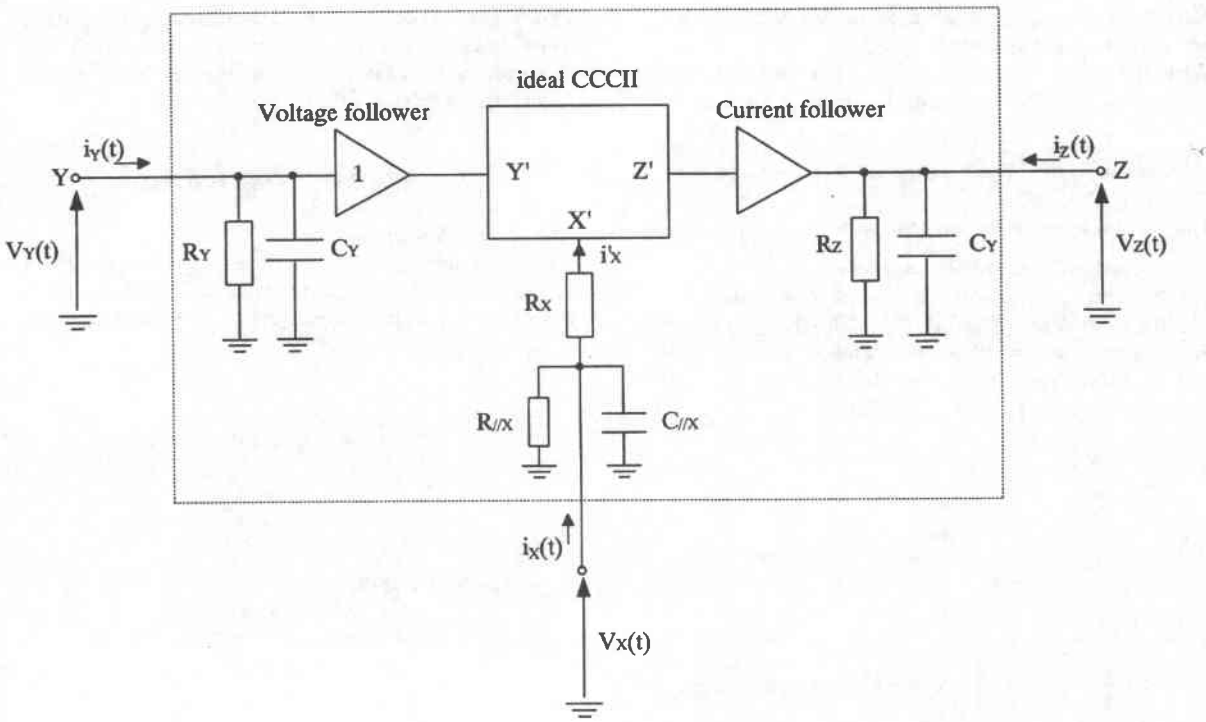


Fig.2: The CMOS CCCII with its parasitic elements.

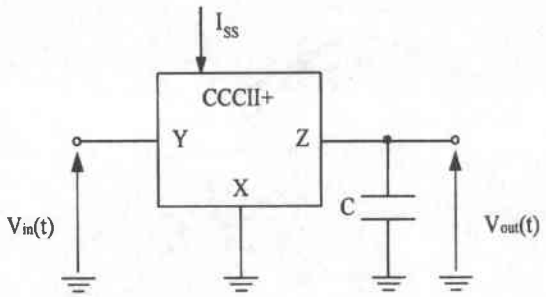


Fig.3: Voltage mode integrator using the CCCII+.

I_{SS}, µA	G_0, dB	f_H, MHz
20	47.4	105.2
50	45	164.3
100	43.3	226
200	41.4	308
300	39.6	355.6

Table2: Variation of the dc gain and the high cut off frequency of the voltage mode integrator as a function of the bias current I_{ss}.

low cut off frequency $f_B = 1/2\pi R_z(C + C_z)$. The unity gain frequency f_0 is $f_0 = 1/2\pi R_x(C + C_z)$.

The frequency response of the integrator in Fig.3 obtained from simulations for I_{ss} = 100µA and C = 3pF, is given in Fig.4. The frequency response of the corresponding ideal integrator has also been indicated in this figure.

From these figures we can see that the right integration domain for the circuit above (C=3pF, I_{ss} = 100µA), assuming a phase tolerance of ± 10° is 2MHz – 36.5MHz. Fig.5 shows the variation of f_B and f_0, with C = 3pF, as a function of the bias current I_{ss} of the conveyor. This also confirms that the time constant of the integrator $\tau = 1/2\pi f_0$ is easily adjustable by varying I_{ss}. Table 2 gives the corresponding values of G_0 and f_H for various values of I_{ss}. We can see that as I_{ss} increases, G_0 decreases meanwhile the high cut off frequency increases.

III.3 Current mode integrator

The current mode integrator function, using a CCCII+, is shown in Fig.6. This act in a similar way as the voltage mode implementation above. As the output current I_{out} is available here at high impedance on port Z, the circuit can directly drive without any buffer, the following stage. Note that, when this circuit is used alone, the input translinear loop of the conveyor can displays some biasing problems. These are due to the input offset current I_{Yoff} at Y, that results from the difference existing between the drain currents of M1 and M3. Indeed, this offset current tends to generate a high DC input voltage, through the parasitic input resistance R_Y. With a high DC voltage at Y, the input translinear loop does not operate correctly inducing weak inversion for some transistors. To remedy this we can either use a DC current source to sink I_{Yoff} or a lower resistance R_{off} in shunt with C.

Nevertheless, using R_{off} leads to some disadvantages like decrease in G_0 and increase in f_B.
When the parasitic elements of the CCCII+ are taken into account, the transfer function of the circuit in Fig.6 is:

$$F_i(s) = \frac{I_{out}}{I_{in}}(s) = -\frac{R_Y}{R_X}\frac{\alpha_0}{1+s/\omega_\alpha}\frac{1}{1+R_Y(C+C_Y)s} \quad (6)$$

This is similar to equation (5), with $G_0 = -R_Y/R_X$, $f_B = 1/2\pi R_Y(C+C_Y)$ and $f_0 = 1/2\pi R_X(C+C_Y)$.
The frequency response of this integrator, with the same conditions as above (C=3pF, I_{ss}=100μA) is shown in Fig.7. Assuming a ± 10° phase tolerance, between ideal and simulated phase response of the integrator, the right integration domain is 2MHz - 19MHz.

This frequency domain is less than the one of the voltage mode integrator. Table 3 gives for this circuit the variations of the characteristic parameters G_0, f_0, f_B and f_H for various values of the bias current.

IV. DIFFERENTATOR FUNCTIONS

IV.1 Ideal differentiator

The differentiator functions operating successively in voltage mode and in current mode will be analyzed in this part. For an ideal differentiator, the transfer function is $G(s) = \tau s$.

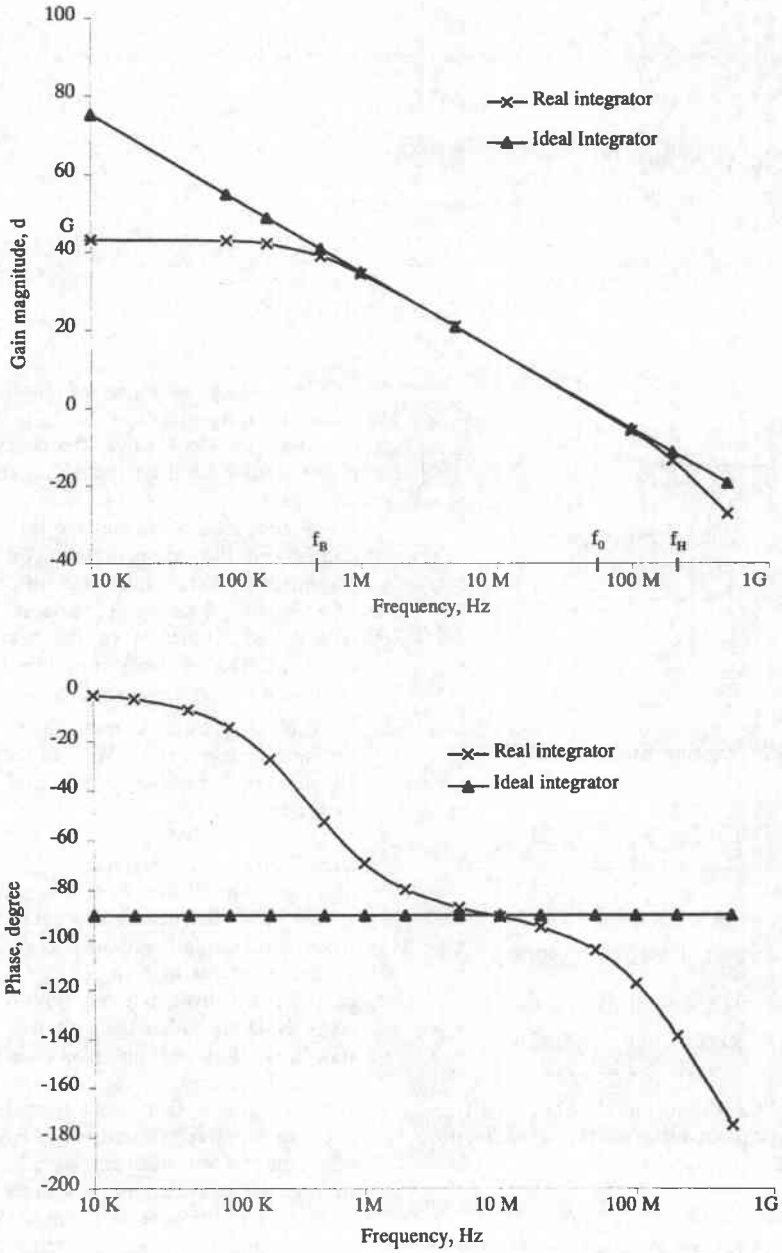


Fig.4: Frequency response of the voltage mode integrator for C=3pF, I_{ss}=100μA, ±3.3V supplies.

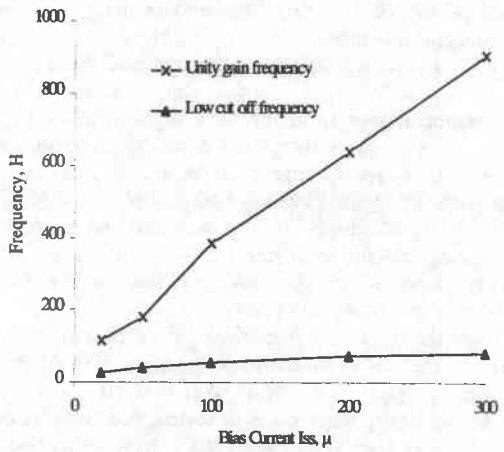


Fig.5: Variation of f_B and f_0 as a function of I_{ss}, for the V-mode integrator, C=3pF, ± 3.3V supplies.

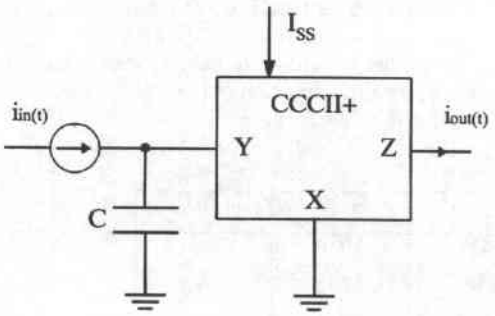


Fig.6: Current mode integrator using the CCCII+.

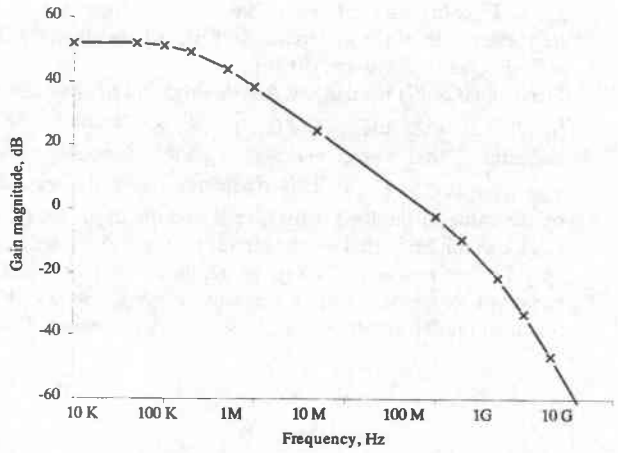
I_{SS}, μA	G_0, dB	f_B, KHz	f_0, MHz	f_H, MHz
20	60.8	40.8	44	129
50	59.3	94.4	70	200
100	52	211	77.8	223
200	46.41	522	103	259
300	40	1200	110	283

Table3: Variation of G_0, f_B, f_0, f_H of the current mode integrator as a function of the bias current I_{ss}.

This is characterized by a low frequency gain equal to zero, a time constant $\tau = R_x C$, a constant phase shift equal to 90° and a unity gain frequency $\omega_\tau = 1/\tau$.

IV.2 Voltage mode differentiator

Fig.8(a) shows the schematic implementation for the voltage mode differentiator using a CCCII+.



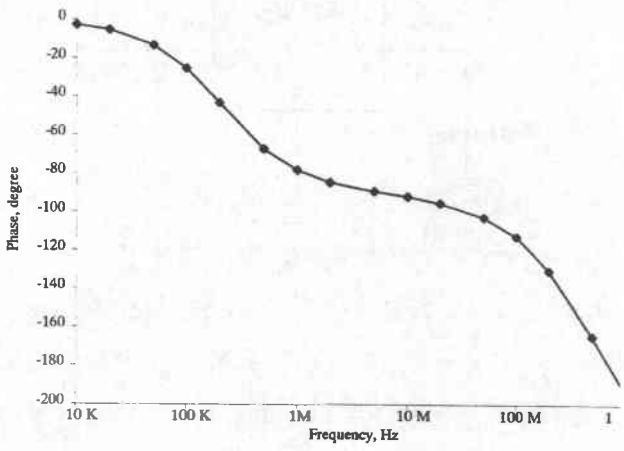
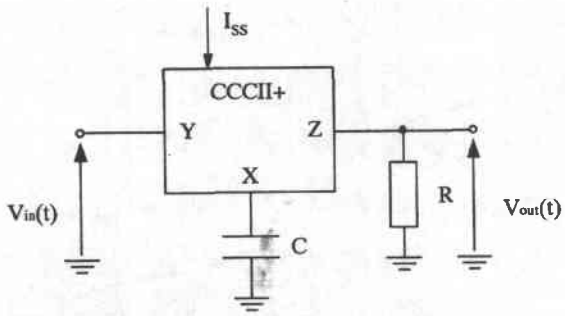


Fig.7: Frequency response of the current mode integrator for C=3pF, I_{ss}=100μA and ± 3.3V supplies.

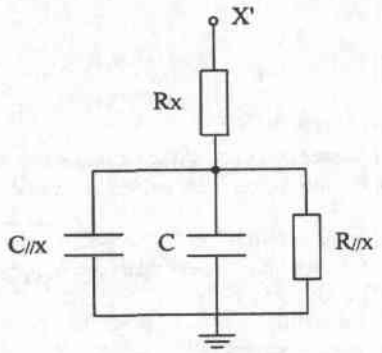
For this implementation, it is necessary that the load resistance R must be lower than the output parasitic resistance R_Z. Also
note that the output voltage must be taken at high impedance using a voltage buffer if necessary.
Fig.8(b) represents the impedance on port X of the conveyor that appears between its intrinsic node X' and ground (see also Fig.1(b) and Fig2). It comprises the parasitic impedances plus the connected capacitor C. All this elements must be considered to understand the frequency response of the two differentiator implementations. From Fig.8(b), we can see that the circuit will be equivalent to $R_{//X}$ at very low frequency, when $f << f_B \approx 1/2\pi R_{//X}(C + C_{//X})$. For $f >> f_B$ it is equivalent to $R_X + 1/((C + C_{//X})s)$.
Now, taking the parasitic elements of the conveyor into account and assuming $R << R_Z$, it follows that the transfer function of the circuit in Fig.8(a), for $f >> f_B$ is:

$$G_v = \frac{\alpha_0}{1 + s/\omega_\alpha} \frac{RCs}{(1 + RC_z s)(1 + R_x(C + C_{//X})s)} \qquad (7)$$

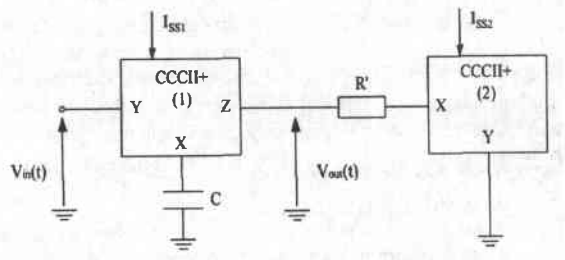
From Fig.8(a) and Fig.8(b), we can see that the low frequency gain of the differentiator for $f<<f_B$ is given by $G_0 = R / R_{//X}$ and the low cut off is f_B.
From equation(7) we can see that the high cut off frequency f_H is $f_H = 1/2\pi R_{//X}(C + C_{//X})$. This equation also indicates that the unity gain frequency is $f_0 = 1/2\pi R(C + C_{//X})$. This frequency that only depends on the value of the load resistance R and the capacitor ($C + C_{//X}$), can not be varied on the circuit in Fig.8(a). In order to vary f_0 electronically, R must be replaced by a controlled conveyor on series with a resistor. Fig.8(c) shows this practical implementation were f_0 is varied by means of I_{ss2}.



(a)



(b)



(c)

Fig.8: Voltage mode differentiator using the CCCII+.
(a) Equivalent circuit.
(b) Effective impedance on port X of the conveyor.
(c) Practical adjustable implementation.

Note that output Z of the second CCCII that must be grounded is not used in this Figure. The design of this CCCII can considerably be reduced to implement port Y and port X only. It must also be noted that one of the most important disadvantages of this differentiator implementation comes from the very high value of $C_{//X}$. Indeed, in the case of an integrated circuit implementation the value of f_B, f_0 and f_H appears to be only dependent on $C_{//X}$, due to the low values available for C (only a few pF).
From the analysis above, we can see that the practical frequency range for differentiator is $f_B - f_H$. This range, that principally depends on $R_{//X}$, $C_{//X}$ and R_X of the first conveyor may be optimized by varying I_{ss1}.
Fig.9 shows the frequency response of the differentiator in Fig.8(a) obtained from simulations for $I_{ss1} = 100\mu A$, $R = 10K\Omega$, and $C = 3pF$. It has also been verified that for $C = 15pF$ the frequency response is unvaried. For comparison purpose the frequency response of the corresponding ideal differentiator has also been added. With a ± 10° phase shift tolerance, the right domain for differentiator is 6KHz – 6.1MHz. In a same way, Fig.10 shows the frequency response obtained with the circuit in Fig.8(c) with $I_{ss1} = 100\mu A$, $I_{ss2} = 100\mu A$ and $C = 3pF$, for various values of R'. Table 4 gives for $R' = 10K\Omega$, the characteristic parameters of the circuit for various values of the bias current I_{ss2}. This demonstrates that I_{ss2} allows to vary f_0 with practically no influence on the differentiation frequency domain.

I_{SS2}, µA	f_B, Hz	f_0, MHz	f_H, MHz
20	1072	4.8	179
50	1092	5	188
100	1081	5.2	192
200	1087	5.3	193
300	1087	5.4	194

Table4: Variation of f_B, f_0, f_H of the voltage mode differentiator as a function of the bias current I_{SS2}, for $R' = 10K\Omega$.

VI.3 Current mode differentiator

Fig.11 shows the theoretical implementation to be used to realize the current mode differentiator. Here, the input I-V conversion resistor R must be lower than the input parasitic resistance R_Y.
For this circuit, the effective impedance on port X of the conveyor is identical to the one in Fig.8(c). It follows that the low cut off frequency f_B has the same value as above $f_B = 1/2\pi R_{//X}(C + C_{//X})$. The transfer function of the circuit in Fig.11, for $f >> f_B$ and assuming $R<<R_Y$ is

$$G_i = \frac{\alpha_0}{1 + s/\omega_\alpha} \frac{R C s}{(1 + R C_Y s)(1 + R_X (C + C_{//X}) s)} \quad (8)$$

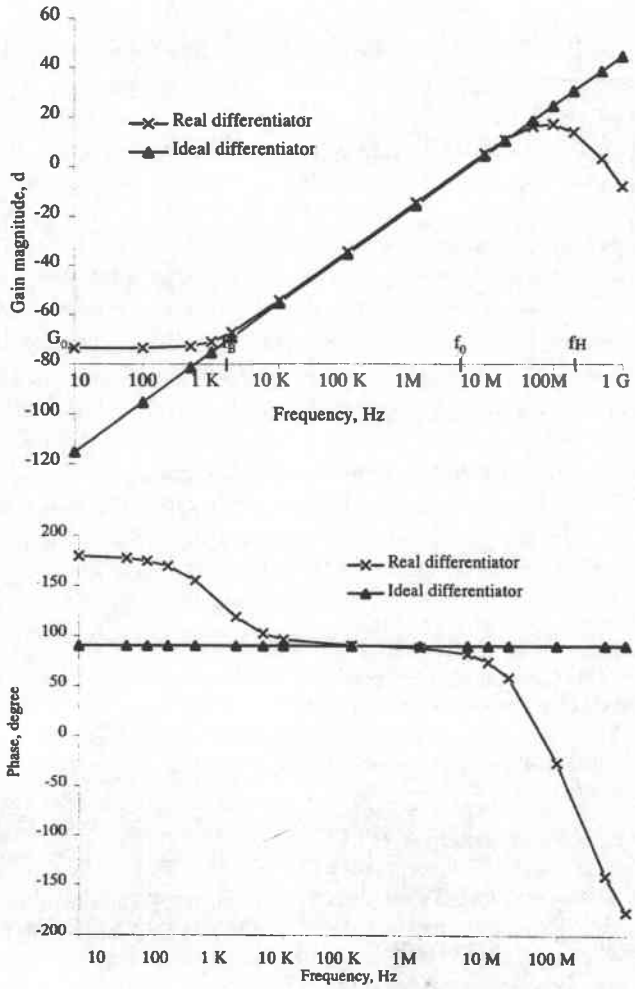


Fig.9: Frequency response of the voltage mode differentiator for C=3pF, $I_{ss1}=I_{ss2}=100\mu A$ and ± 3.3V supplies.

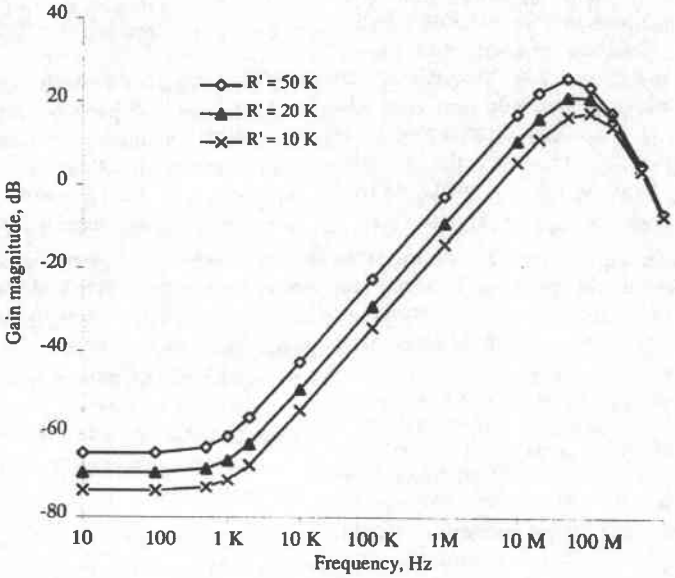


Fig.10: Frequency response of the voltage mode differentiator for various values of R'.

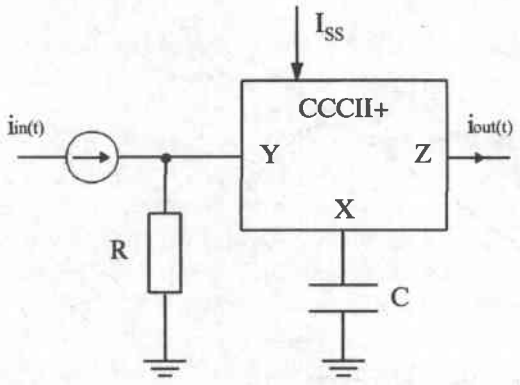


Fig.11: Current mode differentiator using the CCCII+.

Then, it follows that, the characteristics parameters of this differentiator are the same as above:

$G_0=R/R_{//X}$, $f_0 = 1/2\,\pi\,R\,(C+C_{//X})$ and $f_H = 1/2\,\pi\,R_{//X}\,(C+C_{//X})$. Also note the strong dependence of f_B, f_0 and f_H to $C_{//X}$.

Fig.12 shows the frequency response of the differentiator in Fig.11 obtained from simulation for I_{ss1} = 100μA, R = 10KΩ and C = 3pF. It follows that assuming ± 10° phase shift tolerance, the right differentiator domain is 4.9KHz – 4MHz.

As indicated above, R must be replaced by a controlled conveyor in series with a resistor R', to electronically adjust f_0. Also note that the variation domain of f_0 will be lower for the I-mode differentiator for a same bias current. Fig.12 shows the frequency response of the current mode differentiator for C = 3pF, I_{ss} = 100μA and ± 3.3V supplies.

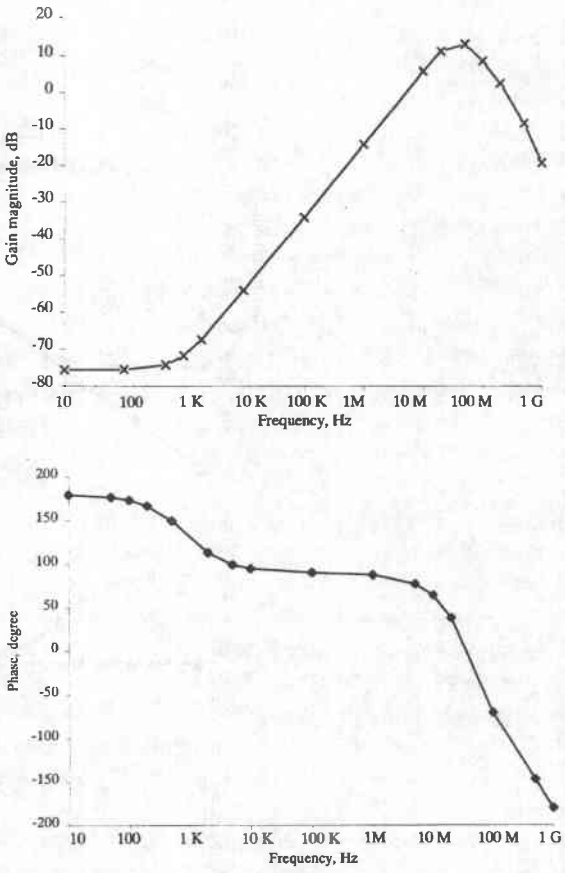


Fig.12: Frequency response of the current mode differentiator for C=3pF, $I_{ss1}=I_{ss2}$ =100μA and ± 3.3V supplies.

V. VARIOUS COMPENSATION METHODS

V.1 General considerations

As shown on the sections above, the limitations for the integrator and differentiator circuits do not result from the same origin. For the integrator implementation, the restrictions that appear at low and very high frequencies (see Fig.4 and Fig.7) can be pushed back using compensation circuits. Indeed, at low frequencies the limitations for $f < f_B$ result from the finite gain value G_0. This value can be increased by artificially increasing either the value of the parasitic output resistance R_Z (V-mode, Fig.3) or the value of R_Y (I-mode, Fig.11). For example, a negative compensation resistance R_{comp}, with $|R_{comp}| > R_{Z,Y}$ allows this increase. The restrictions on the high frequency domain of the integrators circuits, principally result from the high frequency corner f_H of the output current mirrors of the CCCII+. To artificially increase f_H, it is possible to locate a compensation zero at f_H [11].

For the differentiator implementations, it has been shown that two controlled conveyors are necessary to obtain functions with adjustable time constant. The first one implements the differentiator function and the second one the adjustable resistor R (Fig.8(c)). With these differentiators, the high cut off frequency f_H results principally from the high value of the parasitic series resistance R_X of the first conveyor. To increase f_H, it is possible to decrease R_X by using an appropriate design of the CCCII+ [12]. Nevertheless, to decrease the low cut off frequency f_B, that principally depends on the shunt parasitic resistance on X of the first conveyor $R_{//X}$, appears to be more difficult. Indeed, we can only act on the bias current of this conveyor to increase $R_{//X}$.

V.2 Compensation methods for the integrators

V.2.1 Increasing a parasitic resistance

A negative compensation resistance can be connected in parallel to the parasitic resistance $R_{Y,Z}$ (R_Y or R_Z) that must be increased. Fig.13 shows this implementation. The compensation resistance $R_{comp} = -(R_X + R_0)$ is adjustable from the bias current I_{sscomp} of the CCCII+. It is nevertheless necessary that the total equivalent resistance $R_{eq} = R_{Y,Z} // (-(R_X + R_0))$ be positive to preserve the integrator stability. Fig.14 shows, for various values of R_0, the equivalent negative resistance as a function of the bias current of the conveyor.

Note that this negative resistor that principally acts at low frequencies, does not degrade the high frequency behavior of the integrator.

V.2.2 Compensation of the mirror pole

A zero located at f_H must be added to compensate the pole of the output current mirrors. This can be obtained

by adding a resistor rs in series with the capacitor C [11]. The value for rs is given by: $1/2\pi f_H C$.

V.3 Compensation methods for the differentiators

V.3.1 Decreasing R_X

From equations (7,8) we can see that it is necessary to decrease R_X in order to increase f_H. One possibility to decrease R_X, consists of replacing the CCCII by a composite CCCII+ [12]. This configuration consists to add a negative resistor $-\alpha R_X$ (with $\alpha < 1$ and positive) in series with R_X. This leads to very low values for R_X and consequently increase considerably the differentiation frequency range.

V.3.2 Decreasing G_0

It seems to be more difficult to decrease the value of G_0. Indeed noticeable improvements consist in innovative conveyor designs that would be able to exhibit very high values for $R_{//X}$.

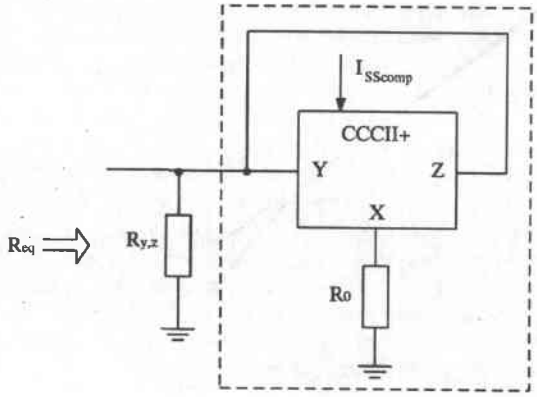


Fig.13: Adjustable negative resistance to increase the shunt parasitic resistance.

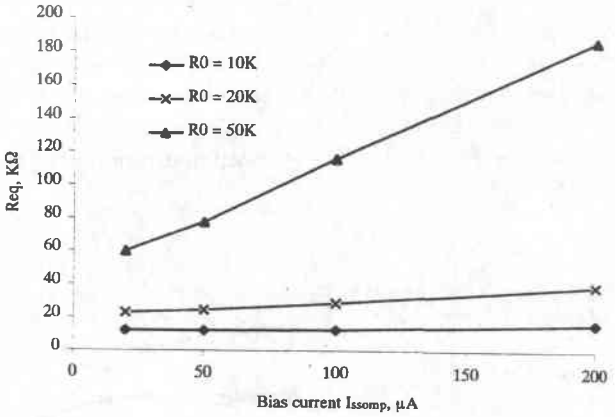


Fig.14: Value of the compensation resistance as a function of I_{sscomp} for differents values of R_0.

VI. COMPENSATED IMPLEMENTATIONS

The voltage mode integrator and differentiator above with their appropriate compensation circuits will be considered in this section in order to fully compare their potentialities.

VI.1 Compensated voltage-mode integrator

Fig.15 shows the practical implementation for the compensated V-mode integrator. As indicated above, R_0 and the second CCCII+ compensate the parasitic output resistance R_Z of the integrator conveyor (CCCII+ number 1). Resistor rs in series with C allows to create a zero that push back the pole effects of the output current mirrors in the same integrator conveyor.

Fig.16 shows the frequency response of the compensated integrator in Fig.15, with the same conditions as above. $I_{ss1} = I_{sscomp} = 100\mu A$, $R_0 = 50K\Omega$, C = 3pF, rs = 240Ω. Note that for simplicity, the same current value was used here to bias the two conveyors. Then the value of R_0 was chosen for right compensation.

In Fig.16 the frequency response of the uncompensated integrator of Fig.4 has also been added to facilitate comparision. Assuming here ± 5° for phase tolerance, we can see in this figure that the right integration frequency domain is 3.7MHz – 21MHz for the uncompensated integrator. This, that becomes 0.9MHz – 140MHz for the compensated one, underlines the efficiency of this approach. In the same way table5 compares the characteristics of both integrator configurations. Varying the conveyor bias current we can see that this compensation also remains efficacious when the integrator time constant is varied.

VI.2 Compensated Voltage-mode differentiator

Fig.17 shows the practical implementation for the compensated V-mode differentiator. Here, the first and the second CCCII+ are used to artificially reduce the resistance R_X of the equivalent composite CCCII+ differentiator. Bias currents I_{ss2} and I_{ss1} must be identical to prevent instability [12].

R and the third CCCII, for which output Z has been suppressed allow to adjust the differentiator time constant. Fig.18 shows the frequency responses of the compensated and uncompensated differentiators above, with $I_{ss} = I_{ss2} = 100\mu A$, C = 3pF, R' = 10KΩ.

Assuming ± 5° phase tolerance, the right differentiator frequency domain are: 12KHz - 3MHz for the uncompensated circuit, and 11KHz - 58MHz for the compensated one.

The improvements that result from the compensation method are evidenced by comparing both frequency ranges. Table6 gives the characteristics of the uncompensated and the compensated differentiators above when the time constant is varied by modifying the value of I_{ss3}.

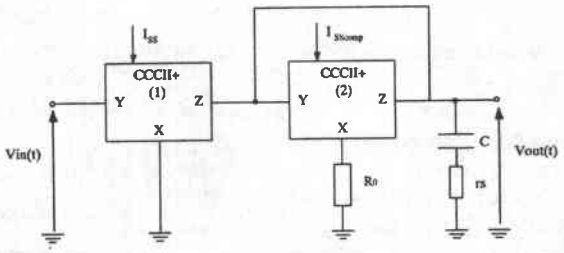
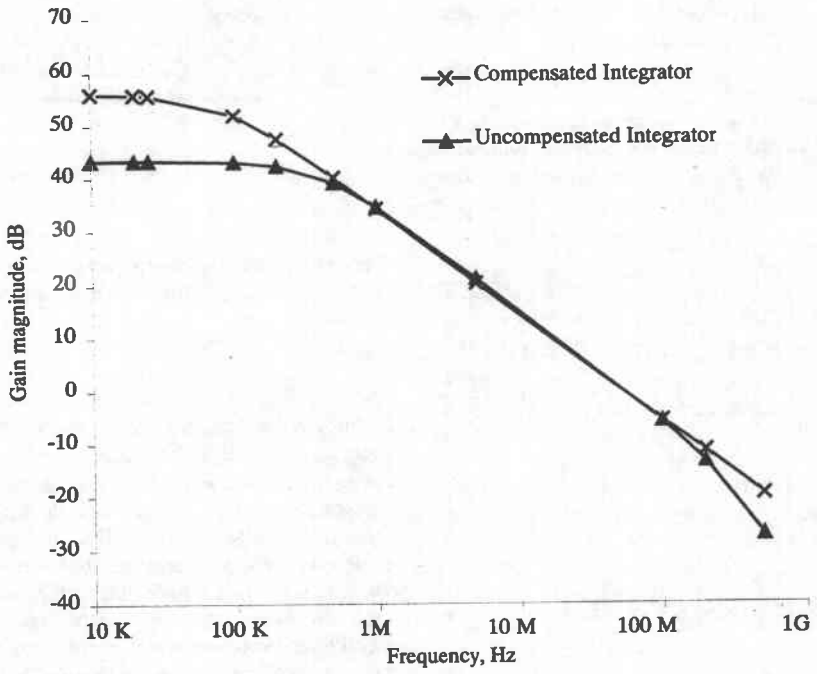


Fig.15: Practical implementation of the compensated voltage mode integrator.



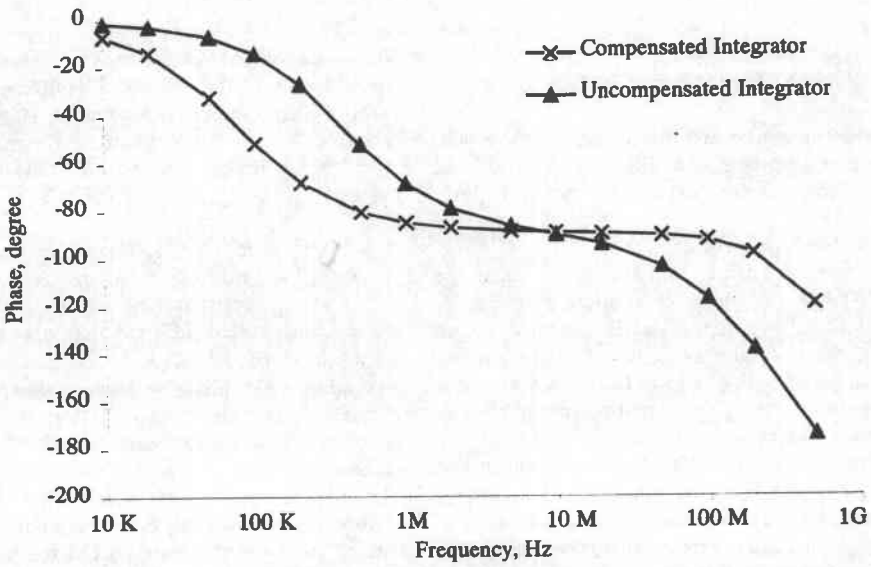


Fig.16: Frequency response of the compensated voltage mode integrator for C=3pF, I_{ss} =100μA and ± 3.3V supplies.

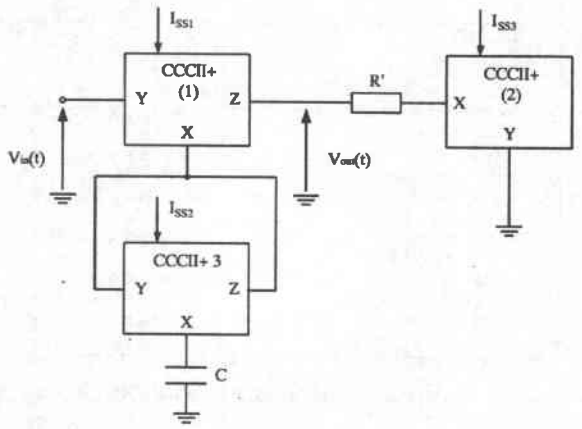


Fig.17: Practical implementation of the compensated voltage mode differentiator.

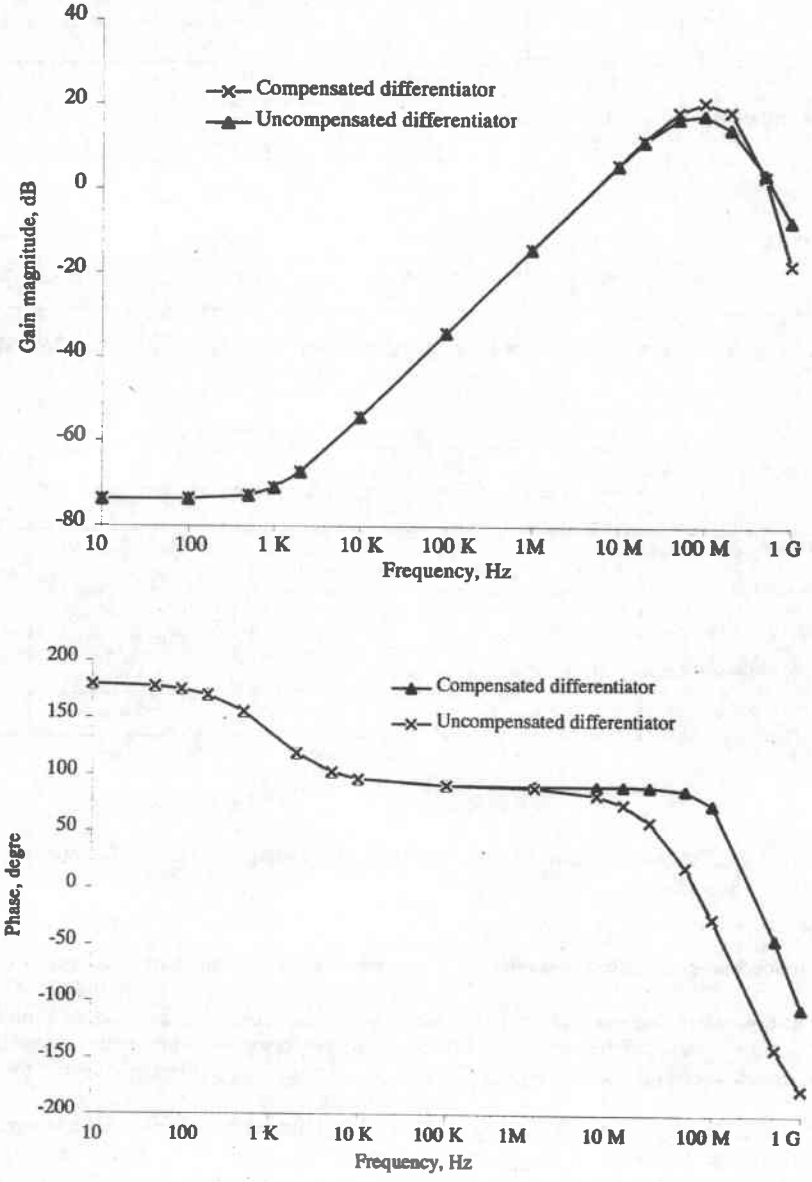


Fig.18: Frequency response of the compensated voltage mode differentiator for C=3pF, $I_{ss1}=I_{ss2}=100\mu A$, 3.3V supplies.

	I_{SS}, μA	G_0, dB	f_0	Right integration domain, ΔΦ=5°, MHz
Uncompensated circuit	80	43.8	49.6	3.1-18.5
	100	43.2	54.7	3.7-21
	120	42.7	59.2	4.1-22.6
Compensated circuit	80	48.7	46.5	1.9-91
	100	56.2	55.5	0.9-140
	120	55	51.2	1.13-183.7

Table5: Performance comparisons for compensated and uncompensated V-mode integrators for various values of I_{ss}.

	I_{SS3}, μA	G_0, dB	f_0, MHz	Right integration domain, ΔΦ=5°, KHz - MHz
Uncompensated circuit	80	-73.54	5.20	12.3 – 3
	100	-73.56	5.22	12.1 – 3.3
	120	-73.58	5.25	12 – 3.8
Compensated circuit	80	-73.62	5.20	12.3 – 57.3
	100	-73.64	5.22	12.1 – 58
	120	-73.66	5.25	12 – 58.6

Table6: Performance comparisons for compensated and uncompensated V-mode differentiators for various values of I_{ss}.

	Integrators		Differentiators	
	V-mode	I-mode	V-mode	I-mode
Versatility	+	+ +	- -	- -
Silicon area	+	+	- -	- -
Frequency range of operation	+ +	+	-	-
High frequency operation	+ +	+ +	- -	- -
Power consumption	+	+	- -	- -

+ + very good, + good, - bad, - - very bad

Table7: Performance comparisons for compensated integrators and differentiators

VIII. Discussion and concluding remarks

It has been shown in this paper that conventional V-mode and I-mode integrator and differentiator circuits implemented from controlled conveyors can beneficially be compensated.

These compensations considerably improve their frequency range for right operation. The differentiator implementation has been found a little less versatile, as the control of the time constant does not directly results from the use of only one controlled conveyor. This implementation has nevertheless been partially improved using a second controlled conveyor to control f_0. As also indicated, the high value of $C_{//X}$ induces serious limitations.

Table7 compares the characteristics of the various compensated implementations for integrators and differentiators.

This indicates for example that integrator circuits must be preferably used when power consumption and accurate operation at high frequency are the most important criterions.

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